EXHIBIT 3

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC. Plaintiff, v. SAMSUNG ELECTRONICS CO., LTD, et al. Defendants.	Civil Case No. 2:22cv00293-JRG (Lead Case) **JURY TRIAL DEMANDED**
NETLIST, INC. Plaintiff, v. MICRON TECHNOLOGY TEXAS, LLC, et al. Defendants.	Civil Case No. 2:22cv-00294-JRG (Member Case) **JURY TRIAL DEMANDED**

DEFENDANTS' P.R. 3-3 INVALIDITY CONTENTIONS

Pursuant to the Docket Control Order in this case (Dkt. 66), agreed amendment thereto (Dkt. 67), and Local Patent Rule 3-3, Defendants Samsung Electronics Co., Ltd. ("SEC") and Samsung Electronics America, Inc. ("SEA") and Samsung Semiconductor, Inc. ("SSI") (collectively, "Samsung") and Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC (collectively, "Micron") (collectively, "Defendants") hereby provide their Invalidity Contentions, which include the accompanying claim charts concerning U.S. Patent Nos. 7,619,912 ("the '912 Patent"); 9,858,215 ("the '215 patent"); and 11,093,417 ("the '417 patent") (collectively, the "Asserted Patents") to Plaintiff Netlist, Inc. ("Plaintiff" or "Netlist").

belief, Netlist's members, including Mr. Bhakta, regularly attended JEDEC meetings for at least the JC-45 committee prior to the priority date of the '912 patent.

By virtue of his attendance at those meetings, active involvement in JEDEC and otherwise, Mr. Bhakta was aware of JEDEC presentations prior to the priority date for the '912 patent such as those related to Fully Buffered DIMM (FBDIMM) presented at the March 8-9, 2005 meeting of JC-45, which Mr. Bhakta attended.

Draft specifications, ballots and presentations distributed to the members of the JC-45 committees of JEDEC were distributed to many (20+) key members of the interested public with the expectation they would be freely disclosed to and discussed with others.

After attending the March 8-9, 2005 meeting and listening to these ideas from other members of JEDEC, Mr. Bhakta returned to Netlist and drafted non-provisional application no. 11/173,175, which provides the earliest possible priority date for the '912 patent given the many deficiencies in the earlier non-provisional and provisional patent disclosures.

With discovery ongoing, Defendants reserve the right to amend, modify, or supplement these Invalidity Contentions with additional 35 U.S.C. §102(f) and/or (g) allegations should additional information become available through discovery supporting such allegations.

B. U.S. Patent Nos. 9,858,215 and 11,093,417

Invalidity claim charts identifying disclosures in the references identified in Tables 1-B, 2-B, 3-B, and 4-B as to the Asserted Claims of the '215 and '417 patents are provided in attached Exhibits B1 through B21 (the '215 Patent) and Exhibits C1 through C18 (the '417 Patent).

Table 1-B: Prior Art Patents and Printed Publications for the '215 and '417 Patents

Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
The '215 Patent's Admitted Prior Art ("APA")		

Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
U.S. Patent Application Publication No. 2003/0204688 ("Lee '688")	10/30/2003	4/25/2003
U.S. Patent Application Publication No. 2006/0117152 ("Amidi")	6/1/2006	1/5/2004
U.S. Patent Application Publication No. 2003/0145156 ("Khandekar")	7/31/2003	1/28/2002
U.S. Patent No. 6,862,653 ("Dodd")	3/1/2005	9/18/2000
U.S. Patent Application Publication No. 2003/0117864 ("Hampel")	6/26/2003	10/22/2002
U.S. Patent No. 7,240,145 ("Holman")	7/3/2007	2/28/2006
U.S. Patent No. 6,757,751 ("Gene")	6/29/2004	8/11/2000
U.S. Patent No. 6,961,281 ("Wong '281")	11/1/2005	9/12/2003
U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119")	8/15/2002	3/13/2002
JEDEC Standards, including without limitation JEDEC Standard JESD79, Double Data Rate (DDR) SDRAM Specification (June 2000) ("JESD79"), JEDEC Standard JESD79-2, DDR SDRAM Specification (September 2003) ("JESD79-2"), JEDEC Standard JESD21-C, PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification (January 2002) ("JESD 21-C"), JEDEC Standard DDR SDRAM Specification, JESD79C (March 2003) ("JESD79C")	June 2002-March 2003	
FBDIMM Architecture & Protocol, including without limitation FB-DIMM Draft Specification: Architecture & Protocol, Revision 0.0 ("*FBDIMM AP Rev. 0.0"*) (December 3, 2003) and FB-DIMM Draft Specification: Architecture & Protocol, Revision 0.1 ("*FBDIMM AP Rev. 0.1"*) (February 13, 2004)	12/3/2003-2/13/2004	
U.S. Patent No. 6,205,062 ("Kim '062")	3/20/2001	11/9/1999
U.S. Patent No. 6,262,938 ("Lee '938")	7/17/2001	3/3/2000
U.S. Patent No. 6,392,909 ("Jang")	5/21/2002	5/27/2001
U.S. Patent No. 6,529,423 ("Yoon")	3/4/2003	2/22/2000
U.S. Patent No. 6,564,287 ("Lee '287")	5/13/2003	9/5/2000
U.S. Patent No. 7,289,383 ("Cornelius")	10/30/2007	8/23/2004
U.S. Patent No. 7,433,258 ("Rao")	10/7/2008	10/8/2004
U.S. Patent No. 5,581,498 ("Ludwig")	12/3/1996	10/20/1994
U.S. Patent No. 5,712,811 ("Kim '811")	1/27/1998	1/6/1996
U.S. Patent No. 5,926,827 ("Dell '827")	7/20/1999	2/9/1996
U.S. Patent No. 6,414,868 ("Wong '868")	7/2/2002	6/7/1999

Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
U.S. Patent No. 6,446,184 ("Dell '184")	9/3/2002	1/30/2001
U.S. Patent No. 6,493,250 ("Halbert '250")	12/10/2002	12/28/2000
U.S. Patent No. 6,529,993 ("Rogers")	3/4/2003	10/12/2000
U.S. Patent No. 6,615,345 ("LaBerge '345")	9/2/2003	7/29/1999
U.S. Patent No. 6,820,163 ("McCall")	11/16/2004	9/18/2000
U.S. Patent No. 7,334,150 ("Ruckerbauer")	2/19/2008	12/3/2004
U.S. Patent No. 7,024,518 ("Halbert '518")	4/4/2006	3/13/2002
U.S. Patent No. 7,043,617 ("Williams '617")	5/9/2006	2/22/2000
U.S. Patent No. 7,092,299 ("Kwak")	8/15/2006	5/3/2004
U.S. Patent No. 7,149,841 ("LaBerge '841")	12/12/2006	3/31/2003
U.S. Patent No. 7,206,896 ("Perego '896")	4/17/2007	4/29/2005
U.S. Patent No. 7,212,424 ("Johnson '424")	5/1/2007	5/21/2005
U.S. Patent No. 7,222,224 ("Woo")	5/22/2007	5/21/2004
U.S. Patent No. 7,363,422 ("Perego '422")	4/22/2008	1/28/2004
U.S. Patent No. 7,366,827 ("Lee '827")	4/29/2008	4/25/2003
U.S. Patent Application Publication No. 2001/0008006 ("Klein")	6/12/2001	2/13/2001
U.S. Patent Application Publication No. 2002/0118578 ("Janzen '578")	8/29/2002	2/23/2001
U.S. Patent Application Publication No. 2002/0188816 ("Johnson '816")	12/12/2002	6/6/2001
U.S. Patent Application Publication No. 2003/0039151 ("Matsui '151")	2/27/2003	8/23/2002
U.S. Patent Application Publication No. 2003/0133331 ("LaBerge '331")	7/17/2003	1/14/2002
U.S. Patent Application Publication No. 2004/0034755 ("LaBerge '755")	2/19/2004	8/16/2002
U.S. Patent Application Publication No. 2005/0050255 ("Jeddeloh")	3/5/2005	8/28/2003
U.S. Patent Application Publication No. 2005/0198449 ("Haskell")	9/8/2005	3/5/2004
U.S. Patent Application Publication No. 2005/0257109 ("Averbuj")	11/17/2005	7/29/2003
U.S. Patent Application Publication No. 2006/0195631 ("Rajamani")	8/31/2006	1/31/2005
U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry")	12/7/2006	6/1/2005
Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Data Sheet, *see* PRIOR_ART-00338461	2002-2004	
Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob)	12/10/2002	
The '417 Patent's Admitted Prior Art ("APA")		

Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
U.S. Patent No. 7,103,742 ("Mailloux")	9/5/2006	12/3/1997
U.S. Patent No. 6,851,032 ("LaBerge '032")	2/1/2005	8/16/2002
U.S. Patent No. 6,154,821 ("Barth")	11/28/2000	3/10/1998
U.S. Patent No. 6,226,755 ("Reeves")	5/1/2001	1/26/1999
U.S. Patent No. 6,742,098 ("Halbert '098")	5/25/2004	10/3/2000
U.S. Patent No. 6,940,782 ("Matsui '782")	9/6/2005	6/13/2003
U.S. Patent No. 7,196,948 ("Vemula")	3/27/2007	3/7/2005
U.S. Patent Application Publication No. 2002/0133666 ("Janzen '666")	9/19/2002	3/13/2001
U.S. Patent Application Publication No. 2004/0103258 ("Blockmon")	5/27/2004	11/27/2002
U.S. Patent Application Publication No. 2004/0260864 ("Lee '864")	12/23/2004	6/19/2003
U.S. Patent Application Publication No. 2005/0044304 ("James")	2/24/2005	8/20/2003
International Patent Application Publication No. WO 96/020446 ("Williams '446")	7/4/1996	12/22/1995
International Patent Application Publication No. WO 01/037090 ("Wong '090")	5/25/2001	11/15/2000
DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C")	January 2002	
DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A")	January 2004	
U.S. Patent. No. 7,155,627 ("Matsui '627")	12/26/2006	8/22/2003
U.S. Patent Application Publication No. 2021/0149829 ("Lee '829")	5/20/2021	12/7/2020

Table 2-B: Prior Art Systems and Inventions for the '215 and '417 Patents

Name of System or Invention	Date of Sale / Offer for Sale / Public Use / Known by Others
Kentron's Quad Band Memory System ("QBM"), *see, e.g.*, PRIOR_ART-00337193; PRIOR_ART-00337196; PRIOR_ART-00337221; PRIOR_ART-00337244; PRIOR_ART-00337259; PRIOR_ART-00337830; PRIOR_ART-00337884; PRIOR_ART-00337910; PRIOR_ART-00337049; and PRIOR_ART-00337512	At least as early as 1999-2005 (sale and/or offer for sale made by Kentron)
DDR3 Functional Outlook, *see, e.g.*, PRIOR_ART-00006576	At least as early as March 2005 (disclosed by Dr. William Wu Shen of Infineon Technologies North America Corp.)

Name of System or Invention	Date of Sale / Offer for Sale / Public Use / Known by Others
Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Products, *see, e.g.*, PRIOR_ART-00338461	At least as early as 2002

For each of the prior art devices identified above, Defendants have listed and produced one or more documents as evidence of the relevant features and functionality. Defendants have obtained or are in the process of obtaining the identified devices and will make them available for inspection. To the extent that one or more documents (*e.g.*, user manual) may be used to describe aspects of a particular device, that device is a single reference for prior art purposes under 35 U.S.C. § 102. Some or all of the corroborating references may also separately qualify as prior art publications under 35 U.S.C. § 102 and may be used as invalidating references under 35 U.S.C. §§ 102 and/or 103.

Further, Defendants are actively searching for information regarding at least the following devices and inventions:

- Kentron's Quad Band Memory System ("QBM")

Discovery is ongoing, and Defendants may serve third parties with document subpoenas. One or more of these devices, along with related documentation, may be invalidating, and Defendants reserve the right to supplement these contentions accordingly.

In addition, Defendants identify, responsive to Plaintiff's infringement contentions, the following patents, publications, and systems as examples of evidence of the state of the art as it relates to memory modules:

- U.S. Patent No. 7,363,422 ("Perego '422");
- U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry");
- U.S. Patent No. 7,024,518 ("Halbert '518");

skill in the art to combine each prior art reference listed in Appendix A with any other reference or references listed in Appendix A along with the knowledge of one of ordinary skill in the art to arrive at the inventions claims in the '912 patent. For example, and without limitation, the Asserted Claims of the '912 patent would have been obvious to one of ordinary skill in the art in view of the following combinations:

Patent No. or Title (Primary Inventor/Author)	**In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))**
The '912 Patent's Admitted Prior Art ("APA")	• U.S. Patent App. Pub. No. 20060117152 ("Amidi") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry") • U.S. Patent No. 7,240,145 ("Holman") • JEDEC Standards • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 5,926,827 ("Dell'827") • U.S. Patent No. 6,209,074 ("Dell'074") • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron's Quad Band Memory System ("QBM") • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 6,742,098 ("Halbert") • U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent No. 7,020,739 ("Mukaida") • U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • U.S. Patent No. 7,414,312 ("Nguyen") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent App. Pub. No. 20060117152 ("Amidi")	• Asserted Patent's Admitted Prior Art ("APA") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry")

	• U.S. Patent No. 7,240,145 ("Holman") • JEDEC Standards • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 5,926,827 ("Dell'827") • U.S. Patent No. 6,209,074 ("Dell'074") • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron's Quad Band Memory System ("QBM") • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 6,742,098 ("Halbert") • U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent No. 7,020,739 ("Mukaida") • U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • U.S. Patent No. 7,414,312 ("Nguyen") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry")	• Asserted Patent's Admitted Prior Art ("APA") • U.S. Patent App. Pub. No. 20060117152 ("Amidi") • U.S. Patent No. 7,240,145 ("Holman") • JEDEC Standards • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 5,926,827 ("Dell'827") • U.S. Patent No. 6,209,074 ("Dell'074") • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron's Quad Band Memory System ("QBM") • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 6,742,098 ("Halbert")

	• U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent No. 7,020,739 ("Mukaida") • U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • U.S. Patent No. 7,414,312 ("Nguyen") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 7,240,145 ("Holman")	• Asserted Patent's Admitted Prior Art ("APA") • U.S. Patent App. Pub. No. 20060117152 ("Amidi") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry") • JEDEC Standards • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 5,926,827 ("Dell'827") • U.S. Patent No. 6,209,074 ("Dell'074") • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron's Quad Band Memory System ("QBM") • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 6,742,098 ("Halbert") • U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent No. 7,020,739 ("Mukaida") • U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • U.S. Patent No. 7,414,312 ("Nguyen") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
JEDEC Standards	• Asserted Patent's Admitted Prior Art ("APA") • U.S. Patent App. Pub. No. 20060117152 ("Amidi") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry")

	• U.S. Patent No. 7,240,145 ("Holman") • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 5,926,827 ("Dell'827") • U.S. Patent No. 6,209,074 ("Dell'074") • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron's Quad Band Memory System ("QBM") • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 6,742,098 ("Halbert") • U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent No. 7,020,739 ("Mukaida") • U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • U.S. Patent No. 7,414,312 ("Nguyen") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 7,363,422 ("Perego '422")	• Asserted Patent's Admitted Prior Art ("APA") • U.S. Patent App. Pub. No. 20060117152 ("Amidi") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry") • U.S. Patent No. 7,240,145 ("Holman") • JEDEC Standards • U.S. Patent No. 5,926,827 ("Dell'827") • U.S. Patent No. 6,209,074 ("Dell'074") • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron's Quad Band Memory System ("QBM") • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 6,742,098 ("Halbert")

	• U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent No. 7,020,739 ("Mukaida") • U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • U.S. Patent No. 7,414,312 ("Nguyen") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 5,926,827 ("Dell'827")	• Asserted Patent's Admitted Prior Art ("APA") • U.S. Patent App. Pub. No. 20060117152 ("Amidi") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry") • U.S. Patent No. 7,240,145 ("Holman") • JEDEC Standards • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 6,209,074 ("Dell'074") • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron's Quad Band Memory System ("QBM") • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 6,742,098 ("Halbert") • U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent No. 7,020,739 ("Mukaida") • U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • U.S. Patent No. 7,414,312 ("Nguyen") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 6,209,074 ("Dell'074")	• Asserted Patent's Admitted Prior Art ("APA") • U.S. Patent App. Pub. No. 20060117152 ("Amidi") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry") • U.S. Patent No. 7,240,145 ("Holman")

	• JEDEC Standards • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 5,926,827 ("Dell'827") • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron's Quad Band Memory System ("QBM") • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 6,742,098 ("Halbert") • U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent No. 7,020,739 ("Mukaida") • U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • U.S. Patent No. 7,414,312 ("Nguyen") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Datasheet	• Asserted Patent's Admitted Prior Art ("APA") • U.S. Patent App. Pub. No. 20060117152 ("Amidi") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry") • U.S. Patent No. 7,240,145 ("Holman") • JEDEC Standards • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 5,926,827 ("Dell'827") • U.S. Patent No. 6,209,074 ("Dell'074") • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron's Quad Band Memory System ("QBM") • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 6,742,098 ("Halbert") • U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent No. 7,020,739 ("Mukaida")

	• U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • U.S. Patent No. 7,414,312 ("Nguyen") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
Micron DDR SDRAM RDIMM, MT36VDDF12872 and/or MT36VDDF25672 Products	• Asserted Patent's Admitted Prior Art ("APA") • U.S. Patent App. Pub. No. 20060117152 ("Amidi") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry") • U.S. Patent No. 7,240,145 ("Holman") • JEDEC Standards • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 5,926,827 ("Dell'827") • U.S. Patent No. 6,209,074 ("Dell'074") • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron's Quad Band Memory System ("QBM") • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 6,742,098 ("Halbert") • U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent No. 7,020,739 ("Mukaida") • U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • U.S. Patent No. 7,414,312 ("Nguyen") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
DDR SDRAM Specification, JDEC Standard No. 79C, March 2003	• Asserted Patent's Admitted Prior Art ("APA") • U.S. Patent App. Pub. No. 20060117152 ("Amidi") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry") • U.S. Patent No. 7,240,145 ("Holman") • JEDEC Standards • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 5,926,827 ("Dell'827") • U.S. Patent No. 6,209,074 ("Dell'074")

	• Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • Kentron's Quad Band Memory System ("QBM") • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 6,742,098 ("Halbert") • U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent No. 7,020,739 ("Mukaida") • U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • U.S. Patent No. 7,414,312 ("Nguyen") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
Kentron's Quad Band Memory System ("QBM")	• Asserted Patent's Admitted Prior Art ("APA") • U.S. Patent App. Pub. No. 20060117152 ("Amidi") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry") • U.S. Patent No. 7,240,145 ("Holman") • JEDEC Standards • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 5,926,827 ("Dell '827") • U.S. Patent No. 6,209,074 ("Dell '074") • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 6,742,098 ("Halbert") • U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent No. 7,020,739 ("Mukaida") • U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • U.S. Patent No. 7,414,312 ("Nguyen") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.

U.S. Patent No. 6,961,281 ("Wong")	• Asserted Patent's Admitted Prior Art ("APA") • U.S. Patent App. Pub. No. 20060117152 ("Amidi") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry") • U.S. Patent No. 7,240,145 ("Holman") • JEDEC Standards • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 5,926,827 ("Dell'827") • U.S. Patent No. 6,209,074 ("Dell'074") • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron's Quad Band Memory System ("QBM") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 6,742,098 ("Halbert") • U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent No. 7,020,739 ("Mukaida") • U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • U.S. Patent No. 7,414,312 ("Nguyen") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 6,996, 686 ("Doblar")	• Asserted Patent's Admitted Prior Art ("APA") • U.S. Patent App. Pub. No. 20060117152 ("Amidi") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry") • U.S. Patent No. 7,240,145 ("Holman") • JEDEC Standards • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 5,926,827 ("Dell '827") • U.S. Patent No. 6,209,074 ("Dell '074") • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003

	• Kentron's Quad Band Memory System ("QBM") • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 6,742,098 ("Halbert") • U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent No. 7,020,739 ("Mukaida") • U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • U.S. Patent No. 7,414,312 ("Nguyen") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 6,757,751 ("Gene")	• Asserted Patent's Admitted Prior Art ("APA") • U.S. Patent App. Pub. No. 20060117152 ("Amidi") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry") • U.S. Patent No. 7,240,145 ("Holman") • JEDEC Standards • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 5,926,827 ("Dell '827") • U.S. Patent No. 6,209,074 ("Dell d'074") • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron's Quad Band Memory System ("QBM") • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,742,098 ("Halbert") • U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent No. 7,020,739 ("Mukaida") • U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • U.S. Patent No. 7,414,312 ("Nguyen") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 6,742,098 ("Halbert")	• Asserted Patent's Admitted Prior Art ("APA")

	• U.S. Patent App. Pub. No. 20060117152 ("Amidi") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry") • U.S. Patent No. 7,240,145 ("Holman") • JEDEC Standards • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 5,926,827 ("Dell '827") • U.S. Patent No. 6,209,074 ("Dell '074") • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron's Quad Band Memory System ("QBM") • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent No. 7,020,739 ("Mukaida") • U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • U.S. Patent No. 7,414,312 ("Nguyen") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 7,181,584 ("LaBerge")	• Asserted Patent's Admitted Prior Art ("APA") • U.S. Patent App. Pub. No. 20060117152 ("Amidi") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry") • U.S. Patent No. 7,240,145 ("Holman") • JEDEC Standards • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 5,926,827 ("Dell'827") • U.S. Patent No. 6,209,074 ("Dell'074") • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003

	• Kentron's Quad Band Memory System ("QBM") • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 6,742,098 ("Halbert") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent No. 7,020,739 ("Mukaida") • U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • U.S. Patent No. 7,414,312 ("Nguyen") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 6,286,077 ("Choi")	• Asserted Patent's Admitted Prior Art ("APA") • U.S. Patent App. Pub. No. 20060117152 ("Amidi") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry") • U.S. Patent No. 7,240,145 ("Holman") • JEDEC Standards • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 5,926,827 ("Dell '827") • U.S. Patent No. 6,209,074 ("Dell '074") • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron's Quad Band Memory System ("QBM") • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 6,742,098 ("Halbert") • U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 7,020,739 ("Mukaida") • U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • U.S. Patent No. 7,414,312 ("Nguyen") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 7,020,739 ("Mukaida")	• Asserted Patent's Admitted Prior Art ("APA")

	• U.S. Patent App. Pub. No. 20060117152 ("Amidi") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry") • U.S. Patent No. 7,240,145 ("Holman") • JEDEC Standards • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 5,926,827 ("Dell'827") • U.S. Patent No. 6,209,074 ("Dell'074") • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron's Quad Band Memory System ("QBM") • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 6,742,098 ("Halbert") • U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • U.S. Patent No. 7,414,312 ("Nguyen") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent App. Pub. No. 2007/0043922 ("Lee")	• Asserted Patent's Admitted Prior Art ("APA") • U.S. Patent App. Pub. No. 20060117152 ("Amidi") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry") • U.S. Patent No. 7,240,145 ("Holman") • JEDEC Standards • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 5,926,827 ("Dell '827") • U.S. Patent No. 6,209,074 ("Dell '074") • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003

	• Kentron's Quad Band Memory System ("QBM") • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 6,742,098 ("Halbert") • U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent No. 7,020,739 ("Mukaida") • U.S. Patent No. 7,414,312 ("Nguyen") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 7,414,312 ("Nguyen")	• Asserted Patent's Admitted Prior Art ("APA") • U.S. Patent App. Pub. No. 20060117152 ("Amidi") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry") • U.S. Patent No. 7,240,145 ("Holman") • JEDEC Standards • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 5,926,827 ("Dell'827") • U.S. Patent No. 6,209,074 ("Dell'074") • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron's Quad Band Memory System ("QBM") • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 6,742,098 ("Halbert") • U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent No. 7,020,739 ("Mukaida") • U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
DDR Functional Outlook	• Asserted Patent's Admitted Prior Art ("APA")

	• U.S. Patent App. Pub. No. 20060117152 ("Amidi") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry") • U.S. Patent No. 7,240,145 ("Holman") • JEDEC Standards • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 5,926,827 ("Dell '827") • U.S. Patent No. 6,209,074 ("Dell '074") • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron's Quad Band Memory System ("QBM") • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 6,742,098 ("Halbert") • U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent No. 7,020,739 ("Mukaida") • U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • U.S. Patent No. 7,414,312 ("Nguyen"); and/or • The knowledge of a person of ordinary skill in the art.

As mentioned above, Defendants have not yet completed their search or discovery concerning additional prior art. Moreover, the exemplary combinations are provided based on Defendants' current understanding of the Asserted Claims and Plaintiff's apparent view of the scope of those claims as shown, for example, in Plaintiff's Infringement Contentions. Further, a *Markman* Order has not yet been issued in this case. As such, Defendants' inclusion of exemplary combinations does not preclude them from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

skill at the time of the alleged invention, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, and it would have been obvious to combine those known elements with the independent claims at least as a matter of common sense and routine innovation. Accordingly, Defendants contend that each Asserted Claim would have been obvious not only by the combinations described in these contentions, but also by any combination of references that renders obvious an Asserted Claim.

In addition to the specific examples of motivation provided above, Defendants reserve the right to rely on the disclosures of the references listed in Appendix B for additional motivation to combine. The above-identified examples of combinations are given merely to illustrate various motivations to combine and are not intended to provide an exhaustive list of every possible combination to which the motivation may apply. Defendants reserve the right to contend that the above-described motivations to combine apply to other combinations at the appropriate time, i.e., in expert reports regarding invalidity.

For at least the reasons described above, it would have been obvious to one of ordinary skill in the art to combine each prior art reference listed in Appendix B with any other reference or references listed in Appendix B along with the knowledge of one of ordinary skill in the art to arrive at the inventions claims in the '215 patent. For example, and without limitation, the Asserted Claims of the '215 patent would have been obvious to one of ordinary skill in the art in view of the following combinations:

Patent No. or Title (Primary Inventor/Author)	**In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))**
The '215 Patent's Admitted Prior Art ("APA")	• U.S. Patent Application Publication No. 2003/0204688 ("Lee '688"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • U.S. Patent Application Publication No.

	2003/0145156 ("Khandekar"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent No. 6,862,653 ("Dodd"); • U.S. Patent Application Publication No. 2003/0117864 ("Hampel"); • U.S. Patent No. 7,240,145 ("Holman"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); • U.S. Patent No. 7,363,422 ("Perego '422"); • JEDEC Standards; • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent Application Publication No. 2005/0198449 ("Haskell"); • FBDIMM Architecture & Protocol; • U.S. Patent No. 6,615,345 ("LaBerge '345"); • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent No. 7,024,518 ("Halbert '518"); • U.S. Patent Application Publication No. 2003/0039151 ("Matsui '151"); • U.S. Patent No. 5,712,811 ("Kim '811"); • U.S. Patent No. 7,334,150 ("Ruckerbauer"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; Kentron's Quad Band Memory System ("QBM"); and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 7,363,422 ("Perego '422")	• JEDEC Standards; • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent No. 7,024,518 ("Halbert '518"); • Kentron's Quad Band Memory System ("QBM");

	• FBDIMM Architecture & Protocol; • U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • U.S. Patent No. 6,862,653 (“Dodd”); • U.S. Patent No. 7,240,145 (“Holman”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • U.S. Patent No. 7,155,627 (“Matsui ’627”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen ’578"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent Publication. No. 2002/0188816 (“Johnson ’816”); • U.S. Patent Application Publication No. 2004/0034755 (“LaBerge ’755”); • U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”);

	• U.S. Patent No. 7,433,258 ("Rao"); • U.S. Pat. No. 5,581,498 ("Ludwig"); • U.S. Patent No. 5,926,827 ("Dell '827"); • DDR3 Functional Outlook; • U.S. Patent Application Publication No. US 2006/0195631 ("Rajamani"); • U.S. Patent Application Publication No. 2005/0198449 ("Haskell"); • U.S. Patent Application Publication No. 2005/0257109 ("Averbuj"); • U.S. Patent No. 6,820,163 ("McCall"); • U.S. Patent No. 7,222,224 ("Woo"); • U.S. Patent No. 7,334,150 ("Ruckerbauer"); • U.S. Patent No. 7,289,383 ("Cornelius"); • U.S. Patent No. 6,392,909 ("Jang"); • U.S. Patent No. 6,529,423 ("Yoon"); • U.S. Patent No. 6,262,938 ("Lee '938"); • U.S. Patent No. 7,206,896 ("Perego '896"); • U.S. Patent No. 6,205,062 ("Kim '062"); • U.S. Patent No. 7,212,424 ("Johnson '424"); and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent Application Publication No. 2003/0204688 ("Lee '688")	• The '215 Patent's Admitted Prior Art ("APA"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • U.S. Patent Application Publication No. 2003/0145156 ("Khandekar"); • DDR3 Functional Outlook; • U.S. Patent No. 6,862,653 ("Dodd"); • U.S. Patent Application Publication No. 2003/0117864 ("Hampel"); • U.S. Patent No. 6,615,345 ("LaBerge '345"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent No. 7,240,145 ("Holman"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • JEDEC Standards; • DDR3 Functional Outlook; • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • Kentron's Quad Band Memory System ("QBM");

	• FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF2672 Product; • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • U.S. Patent Publication. No. 2002/0188816 (“Johnson ’816”); • U.S. Patent No. 6,414,868 (“Wong ’868”); • U.S. Patent Application Publication No. 2004/0034755 (“LaBerge ’755”); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 6,392,909 (“Jang”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 6,529,423 (“Yoon”);

	• U.S. Patent No. 6,564,287 ("Lee '287"); • U.S. Patent No. 6,262,938 ("Lee '938"); • U.S. Patent No. 7,366,827 ("Lee '827"); • U.S. Patent No. 7,212,424 ("Johnson '424"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent Application Publication No. 2006/0117152 ("Amidi")	• The '215 Patent's Admitted Prior Art ("APA"); • U.S. Patent Application Publication No. 2003/0204688 ("Lee '688"); • U.S. Patent Application Publication No. 2003/0145156 ("Khandekar"); • DDR3 Functional Outlook; • U.S. Patent No. 6,862,653 ("Dodd"); • U.S. Patent Application Publication No. 2003/0117864 ("Hampel"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent No. 7,240,145 ("Holman"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • FBDIMM Architecture & Protocol; • U.S. Patent No. 7,206,896 ("Perego '896"); • JEDEC Standards; • U.S. Patent No. 6,615,345 ("LaBerge '345"); • U.S. Patent No. 7,222,224 ("Woo"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • Kentron's Quad Band Memory System ("QBM"); • U.S. Patent No. 7,433,258 ("Rao"); • U.S. Pat. No. 5,581,498 ("Ludwig"); • U.S. Patent No. 7,043,617 ("Williams '617"); • U.S. Patent No. 6,529,993 ("Rogers"); • U.S. Patent No. 5,926,827 ("Dell '827"); • U.S. Patent Application Publication No. 2005/0257109 ("Averbuj"); • U.S. Patent Application Publication No. US 2006/0195631 ("Rajamani"); • U.S. Patent No. 5,712,811 ("Kim '811"); • U.S. Patent No. 6,414,868 ("Wong '868");

	• Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 7,363,422 ("Perego '422"); • JEDEC Standards; • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent No. 7,024,518 ("Halbert '518"); • U.S. Patent Application Publication No. 2003/0039151 ("Matsui '151"); • U.S. Patent No. 6,820,163 ("McCall"); • U.S. Patent Application Publication No. 2005/0198449 ("Haskell");; • U.S. Patent Publication. No. 2002/0188816 ("Johnson '816"); • U.S. Patent No. 7,334,150 ("Ruckerbauer"); • U.S. Patent No. 7,092,299 B2 ("Kwak"); • U.S. Patent No. 7,289,383 ("Cornelius"); • U.S. Patent No. 7,149,841 ("LaBerge '841"); • U.S. Patent No. 6,564,287 ("Lee '287"); • U.S. Patent No. 6,262,938 ("Lee '938"); • U.S. Patent No. 7,366,827 ("Lee '827"); • U.S. Patent No. 7,212,424 ("Johnson '424"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent Application Publication No. 2003/0145156 ("Khandekar")	• The '215 Patent's Admitted Prior Art ("APA"); • U.S. Patent Application Publication No. 2003/0204688 ("Lee '688"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • U.S. Patent No. 6,862,653 ("Dodd"); • U.S. Patent Application Publication No. 2003/0117864 ("Hampel"); • U.S. Patent No. 7,240,145 ("Holman"); • DDR3 Functional Outlook; • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • JEDEC Standards;

	• DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • Kentron's Quad Band Memory System ("QBM"); • U.S. Patent No. 7,149,841 ("LaBerge '841") • U.S. Patent No. 7,363,422 ("Perego '422"); • JEDEC Standards; • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent No. 7,024,518 ("Halbert '518"); • U.S. Patent Application Publication No. 2003/0039151 ("Matsui '151"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent Publication. No. 2002/0188816 ("Johnson '816"); • U.S. Patent No. 6,615,345 ("LaBerge '345"); • U.S. Patent Application Publication No. 2004/0034755 ("LaBerge '755"); • U.S. Patent No. 7,222,224 ("Woo"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent Application Publication No. 2003/0133331 ("LaBerge '331") • U.S. Patent No. 7,206,896 ("Perego '896"); U.S. Patent No. 6,414,868 ("Wong '868"); • U.S. Patent No. 7,433,258 ("Rao"); • U.S. Patent No. 7,043,617 ("Williams '617"); • U.S. Pat. No. 5,581,498 ("Ludwig"); • U.S. Patent No. 5,926,827 ("Dell '827"); • U.S. Patent Application Publication No. 2005/0257109 ("Averbuj"); • U.S. Patent No. 6,529,993 ("Rogers"); • U.S. Patent Application Publication No. US 2006/0195631 ("Rajamani"); • U.S. Patent No. 6,820,163 ("McCall"); • U.S. Patent Application Publication No. 2005/0198449 ("Haskell");

	• U.S. Patent No. 7,334,150 ("Ruckerbauer"); • U.S. Patent No. 6,564,287 ("Lee '287"); • U.S. Patent No. 7,092,299 ("Kwak"); • U.S. Patent No. 5,712,811 ("Kim '811"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); and/or • The knowledge of a person of ordinary skill in the art. The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 6,862,653 ("Dodd")	• The '215 Patent's Admitted Prior Art ("APA"); • U.S. Patent Application Publication No. 2003/0204688 ("Lee '688"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • U.S. Patent Application Publication No. 2003/0145156 ("Khandekar"); • DDR3 Functional Outlook; • U.S. Patent Application Publication No. 2003/0117864 ("Hampel"); • FBDIMM Architecture & Protocol; • U.S. Patent No. 7,240,145 ("Holman"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • Kentron's Quad Band Memory System ("QBM"); • U.S. Patent No. 7,363,422 ("Perego '422"); • JEDEC Standards; • U.S. Patent No. 6,615,345 ("LaBerge '345"); • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent No. 5,712,811 ("Kim '811"); • U.S. Patent No. 7,024,518 ("Halbert '518") • U.S. Patent Application Publication No. 2003/0039151 ("Matsui '151"); • U.S. Patent No. 7,149,841 ("LaBerge '841"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies

	(Bruce Jacob); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 7,206,896 ("Perego '896"); • U.S. Patent No. 7,212,424 ("Johnson '424"); • U.S. Patent No. 7,366,827 ("Lee '827"); • U.S. Patent No. 6,446,184 ("Dell '184"); • U.S. Patent No. 6,414,868 ("Wong '868"); • U.S. Patent No. 6,205,062 ("Kim '062"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent No. 5,926,827 ("Dell '827"); • U.S. Patent Application Publication No. 2005/0257109 ("Averbuj"); • U.S. Patent No. 6,564,287 ("Lee '287"); • U.S. Patent Application Publication No. 2004/0034755 ("LaBerge '755"); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen '578"); • U.S. Patent Application Publication No. 2005/0198449 ("Haskell"); • U.S. Patent No. 7,222,224 ("Woo"); • U.S. Patent No. 7,334,150 ("Ruckerbauer"); • U.S. Patent Application Publication No. 2003/0133331 ("LaBerge '331"); • U.S. Patent No. 7,092,299 ("Kwak"); U.S. Patent Application Publication No. 2005/0050255 ("Jeddeloh"); and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 7,240,145 ("Holman")	• The '215 Patent's Admitted Prior Art ("APA"); • U.S. Patent Application Publication No. 2003/0204688 ("Lee '688"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • DDR3 Functional Outlook; • U.S. Patent No. 6,615,345 ("LaBerge '345"); • U.S. Patent Application Publication No. 2003/0145156 ("Khandekar"): • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent No. 6,862,653 ("Dodd");

	• U.S. Patent Application Publication No. 2003/0117864 (“Hampel”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • JEDEC Standards; • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • FBDIMM Architecture & Protocol; • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • Kentron’s Quad Band Memory System (“QBM”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 7,206,896 (“Perego ’896”) • U.S. Patent No. 7,366,827 (Lee ’827); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 6,414,868 (“Wong ’868”); • U.S. Patent No. 6,205,062 ("Kim ’062"); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent Application Publication No. 2004/0034755 (“LaBerge ’755”); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen ’578"); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”);

	• U.S. Patent Application Publication No. 2003/0133331 ("LaBerge '331"); • U.S. Patent No. 7,092,299 ("Kwak"); • U.S. Patent Application Publication No. 2005/0050255 ("Jeddeloh"); and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent Application Publication No. 2003/0117864 ("Hampel")	• The '215 Patent's Admitted Prior Art ("APA"); • U.S. Patent Application Publication No. 2003/0204688 ("Lee '688"); • DDR3 Functional Outlook; • U.S. Patent No. 6,446,184 ("Dell '184"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • U.S. Patent Application Publication No. 2003/0145156 ("Khandekar"); • U.S. Patent No. 6,862,653 ("Dodd"); • U.S. Patent No. 6,820,163 ("McCall"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent No. 7,240,145 ("Holman"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); • JEDEC Standards; • U.S. Patent Application Publication No. US 2006/0195631 ("Rajamani"); • FBDIMM Architecture & Protocol; • U.S. Patent No. 6,615,345 ("LaBerge '345"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • Kentron's Quad Band Memory System ("QBM"); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 7,043,617 ("Williams '617"); • U.S. Patent No. 7,206,896 ("Perego '896") • U.S. Patent No. 6,529,423 ("Yoon"); • U.S. Patent No. 6,564,287 ("Lee '287");

	• U.S. Patent No. 7,433,258 (“Rao”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,392,909 (“Jang”); • U.S. Patent No. 6,262,938 (“Lee ’938”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 6,205,062 ("Kim ’062"); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen ’578"); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Publication. No. 2002/0188816 (“Johnson ’816”); • U.S. Patent No. 6,414,868 (“Wong ’868”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent Application Publication No. 2004/0034755 (“LaBerge ’755”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 7,024,518 (“Halbert ’518”) • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (Lee ’827); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”)	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”);

	• DDR3 Functional Outlook; • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • U.S. Patent No. 6,862,653 (“Dodd”); • U.S. Patent Application Publication No. 2003/0117864 (“Hampel”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 6,493,250 (“Halbert ’250”); • JEDEC Standards; • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent Publication. No. 2002/0188816 (“Johnson ’816”); • U.S. Patent No. 7,092,299 (“Kwak”);U.S. Patent No. 7,206,896 (Perego ’896) • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 6,205,062 ("Kim ’062"); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen ’578"); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob);

	• U.S. Patent No. 6,615,345 ("LaBerge '345"); • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent No. 7,024,518 ("Halbert '518") • U.S. Patent Application Publication No. 2003/0039151 ("Matsui '151"); • U.S. Patent No. 7,043,617 ("Williams '617"); • U.S. Patent No. 7,433,258 ("Rao"); • U.S. Patent No. 7,289,383 ("Cornelius"); • U.S. Patent No. 6,262,938 ("Lee '938"); • U.S. Patent No. 7,212,424 ("Johnson '424"); • U.S. Patent No. 7,366,827 (Lee '827); • Kentron's Quad Band Memory System ("QBM"); and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 7,024,518 ("Halbert '518")	• The '215 Patent's Admitted Prior Art ("APA"); • U.S. Patent Application Publication No. 2003/0204688 ("Lee '688"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • FBDIMM Architecture & Protocol; • DDR3 Functional Outlook; • U.S. Patent Application Publication No. 2003/0145156 ("Khandekar"); • U.S. Patent No. 6,862,653 ("Dodd"); • U.S. Patent Application Publication No. 2003/0117864 ("Hampel"); • U.S. Patent No. 7,240,145 ("Holman"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 6,493,250 ("Halbert '250"); • JEDEC Standards; • U.S. Patent No. 7,334,150 ("Ruckerbauer"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • U.S. Patent Publication. No. 2002/0188816

	("Johnson '816"); • U.S. Patent No. 7,092,299 ("Kwak");U.S. Patent No. 7,206,896 (Perego '896) • U.S. Patent No. 6,529,423 ("Yoon"); • U.S. Patent No. 6,564,287 ("Lee '287"); • U.S. Patent No. 7,222,224 ("Woo"); • U.S. Patent No. 5,712,811 ("Kim '811"); • U.S. Patent No. 6,205,062 ("Kim '062"); • U.S. Patent No. 5,926,827 ("Dell '827"); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen '578"); • U.S. Patent Application Publication No. 2005/0198449 ("Haskell"); • U.S. Patent Application Publication No. 2003/0133331 ("LaBerge '331"); • U.S. Patent Application Publication No. 2005/0257109 ("Averbuj"); • U.S. Patent Application Publication No. 2005/0050255 ("Jeddeloh"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,615,345 ("LaBerge '345"); • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • U.S. Patent Application Publication No. 2003/0039151 ("Matsui '151"); • U.S. Patent No. 7,043,617 ("Williams '617"); • U.S. Patent No. 7,433,258 ("Rao"); • U.S. Patent No. 7,289,383 ("Cornelius"); • U.S. Patent No. 6,262,938 ("Lee '938"); • U.S. Patent No. 7,212,424 ("Johnson '424"); • U.S. Patent No. 7,366,827 (Lee '827); • Kentron's Quad Band Memory System ("QBM"); and/or • The knowledge of a person of ordinary skill in the art.
DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C")	• The '215 Patent's Admitted Prior Art ("APA"); • U.S. Patent Application Publication No. 2003/0204688 ("Lee '688"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi");

	• DDR3 Functional Outlook; • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2003/0145156 ("Khandekar"); • U.S. Patent No. 6,862,653 ("Dodd"); • U.S. Patent Application Publication No. 2003/0117864 ("Hampel"); • U.S. Patent No. 7,240,145 ("Holman"); • U.S. Patent No. 5,712,811 ("Kim '811"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent Application Publication No. 2005/0198449 ("Haskell"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • U.S. Patent No. 7,334,150 ("Ruckerbauer"); • U.S. Patent No. 7,366,827 (Lee '827); • U.S. Patent No. 7,043,617 ("Williams '617"); • U.S. Patent No. 7,433,258 ("Rao"); • U.S. Patent No. 7,289,383 ("Cornelius"); • U.S. Patent No. 6,262,938 ("Lee '938"); • U.S. Patent No. 7,149,841 ("LaBerge '841"); • U.S. Patent No. 7,206,896 (Perego '896); • U.S. Patent No. 6,564,287 ("Lee '287"); • U.S. Patent No. 5,926,827 ("Dell '827"); • U.S. Patent No. 7,222,224 ("Woo"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); • U.S. Patent No. 6,615,345 ("LaBerge '345"); • U.S. Patent No. 7,363,422 ("Perego '422"); • JEDEC Standards; • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • U.S. Patent Publication. No. 2002/0188816 ("Johnson '816"); • U.S. Patent No. 7,092,299 ("Kwak"); • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent No. 7,024,518 ("Halbert '518")

	• U.S. Patent Application Publication No. 2003/0039151 ("Matsui '151"); • Kentron's Quad Band Memory System ("QBM"); and/or • The knowledge of a person of ordinary skill in the art.
DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A")	• The '215 Patent's Admitted Prior Art ("APA"); • U.S. Patent Application Publication No. 2003/0204688 ("Lee '688"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • DDR3 Functional Outlook; • U.S. Patent Application Publication No. 2003/0145156 ("Khandekar"); • U.S. Patent No. 6,862,653 ("Dodd"); • U.S. Patent Application Publication No. 2003/0117864 ("Hampel"); • U.S. Patent No. 7,240,145 ("Holman"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); • U.S. Patent No. 6,564,287 ("Lee '287"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 6,615,345 ("LaBerge '345"); • U.S. Patent No. 7,212,424 ("Johnson '424"); • U.S. Patent No. 7,334,150 ("Ruckerbauer"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent No. 7,363,422 ("Perego '422"); • JEDEC Standards; • U.S. Patent No. 5,926,827 ("Dell '827"); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen '578"); • U.S. Patent Application Publication No. 2005/0198449 ("Haskell");

	• U.S. Patent Application Publication No. 2003/0133331 ("LaBerge '331"); • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent No. 7,222,224 ("Woo"); • U.S. Patent No. 7,024,518 ("Halbert '518") • U.S. Patent Application Publication No. 2003/0039151 ("Matsui '151"); • U.S. Patent No. 5,712,811 ("Kim '811"); • Kentron's Quad Band Memory System ("QBM"); and/or • The knowledge of a person of ordinary skill in the art.
JEDEC Standards	• The '215 Patent's Admitted Prior Art ("APA"); • U.S. Patent Application Publication No. 2003/0204688 ("Lee '688"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • DDR3 Functional Outlook; • U.S. Patent Application Publication No. 2003/0145156 ("Khandekar"); • U.S. Patent No. 6,862,653 ("Dodd"); • U.S. Patent Application Publication No. 2003/0117864 ("Hampel"); • U.S. Patent No. 6,615,345 ("LaBerge '345"); • U.S. Patent No. 7,240,145 ("Holman"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • Kentron's Quad Band Memory System ("QBM"); • FBDIMM Architecture & Protocol; • U.S. Patent No. 7,206,896 ("Perego '896"); • U.S. Patent No. 6,529,423 ("Yoon"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 7,155,627 ("Matsui '627"); • U.S. Patent No. 7,334,150 ("Ruckerbauer");

	• U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen ’578"); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent No. 6,262,938 (“Lee ’938”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 6,205,062 ("Kim ’062"); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent No. 7,024,518 (“Halbert ’518”) • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 7,366,827 (Lee ’827); and/or • The knowledge of a person of ordinary skill in the art.
Kentron’s Quad Band Memory System (“QBM”)	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • DDR3 Functional Outlook; • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • U.S. Patent No. 6,862,653 (“Dodd”); • U.S. Patent Application Publication No. 2003/0117864 (“Hampel”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • JEDEC Standards;

	• FBDIMM Architecture & Protocol; • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 7,206,896 (“Perego ’896”) • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent No. 6,262,938 (“Lee ’938”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 6,205,062 ("Kim ’062"); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen ’578"); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 7,024,518 (“Halbert ’518”) • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 7,366,827 (Lee ’827); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”)	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No.

	2006/0117152 (“Amidi”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • U.S. Patent No. 6,862,653 (“Dodd”); • U.S. Patent Application Publication No. 2003/0117864 (“Hampel”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • JEDEC Standards; • FBDIMM Architecture & Protocol; • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • DDR3 Functional Outlook; • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent Publication. No. 2002/0188816 (“Johnson ’816”); • U.S. Patent No. 7,092,299 (“Kwak”); • Kentron’s Quad Band Memory System (“QBM”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 6,529,993 ("Rogers"); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen ’578"); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”);

	• U.S. Patent No. 5,712,811 ("Kim '811"); • U.S. Patent No. 6,414,868 ("Wong '868"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 6,564,287 ("Lee '287"); • U.S. Patent No. 7,222,224 ("Woo"); • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); • U.S. Patent Application Publication No. 2003/0039151 ("Matsui '151"); and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 6,493,250 ("Halbert '250")	• The '215 Patent's Admitted Prior Art ("APA"); • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • DDR3 Functional Outlook; • U.S. Patent Application Publication No. 2003/0204688 ("Lee '688"); • U.S. Patent Application Publication No. 2003/0145156 ("Khandekar"); • U.S. Patent No. 6,862,653 ("Dodd"); • U.S. Patent Application Publication No. 2003/0117864 ("Hampel"); • U.S. Patent No. 7,240,145 ("Holman"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • U.S. Patent No. 7,334,150 ("Ruckerbauer"); • JEDEC Standards; • FBDIMM Architecture & Protocol; • U.S. Patent No. 6,615,345 ("LaBerge '345"); • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent No. 7,024,518 ("Halbert '518"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C");

	• DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • U.S. Patent Publication. No. 2002/0188816 ("Johnson '816"); • U.S. Patent No. 7,092,299 ("Kwak"); • Kentron's Quad Band Memory System ("QBM"); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 7,043,617 ("Williams '617"); • U.S. Patent No. 7,366,827 (Lee '827); • U.S. Patent No. 7,289,383 ("Cornelius"); • U.S. Patent No. 6,262,938 ("Lee '938"); • U.S. Patent No. 6,564,287 ("Lee '287"); • U.S. Patent No. 7,222,224 ("Woo"); • U.S. Patent No. 7,433,258 ("Rao"); • U.S. Patent No. 6,529,993 ("Rogers"); • U.S. Pat. No. 5,581,498 ("Ludwig"); • U.S. Patent No. 5,926,827 ("Dell '827"); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen '578"); • U.S. Patent Application Publication No. 2005/0198449 ("Haskell"); • U.S. Patent Application Publication No. 2003/0133331 ("LaBerge '331"); • U.S. Patent Application Publication No. 2005/0257109 ("Averbuj"); • U.S. Patent Application Publication No. US 2006/0195631 ("Rajamani"); • U.S. Patent No. 5,712,811 ("Kim '811"); • U.S. Patent No. 6,414,868 ("Wong '868"); • U.S. Patent No. 7,149,841 ("LaBerge '841"); • U.S. Patent No. 7,206,896 ("Perego '896"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein") • U.S. Patent Application Publication No. 2003/0039151 ("Matsui '151"); and/or • The knowledge of a person of ordinary skill in the art.

U.S. Patent Application Publication No. 2001/0008006 (“Klein”)	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 6,862,653 (“Dodd”); • DDR3 Functional Outlook; • U.S. Patent Application Publication No. 2003/0117864 (“Hampel”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • JEDEC Standards; • FBDIMM Architecture & Protocol; • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • U.S. Patent No. 7,155,627 (“Matsui ’627”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent Publication. No. 2002/0188816 (“Johnson ’816”); • Kentron’s Quad Band Memory System (“QBM”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 6,529,993 ("Rogers"); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen ’578"); • U.S. Patent Application Publication No.

	2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 6,414,868 (“Wong ’868”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); and/or • The knowledge of a person of ordinary skill in the art.
DDR3 Functional Outlook	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • JEDEC Standards; • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • Kentron’s Quad Band Memory System (“QBM”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • FBDIMM Architecture & Protocol; • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”);

	• U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • U.S. Patent No. 6,862,653 (“Dodd”); • U.S. Patent No. 7,240,145 (“Holman”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • U.S. Patent No. 7,155,627 (“Matsui ’627”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen ’578"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent Publication. No. 2002/0188816 (“Johnson ’816”); • U.S. Patent Application Publication No. 2004/0034755 (“LaBerge ’755”); • U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 6,820,163 (“McCall”); • U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,392,909 (“Jang”); • U.S. Patent No. 6,529,423 (“Yoon”);

	• U.S. Patent No. 6,262,938 ("Lee '938"); • U.S. Patent No. 7,206,896 ("Perego '896"); • U.S. Patent No. 6,205,062 ("Kim '062"); • U.S. Patent No. 7,212,424 ("Johnson '424"); and/or • The knowledge of a person of ordinary skill in the art.
FBDIMM Architecture & Protocol	• The '215 Patent's Admitted Prior Art ("APA"); • U.S. Patent No. 7,363,422 ("Perego '422"); • JEDEC Standards; • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent No. 7,024,518 ("Halbert '518"); • Kentron's Quad Band Memory System ("QBM"); • DDR3 Functional Outlook; • U.S. Patent No. 6,615,345 ("LaBerge '345"); • U.S. Patent Application Publication No. 2003/0039151 ("Matsui '151"); • U.S. Patent No. 5,712,811 ("Kim '811"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • U.S. Patent No. 7,212,424 ("Johnson '424"); • U.S. Patent No. 7,149,841 ("LaBerge '841"); • U.S. Patent No. 7,366,827 ("Lee '827"); • U.S. Patent Application Publication No. 2003/0204688 ("Lee '688"); • U.S. Patent Application Publication No. 2003/0145156 ("Khandekar"); • U.S. Patent No. 6,862,653 ("Dodd"); • U.S. Patent No. 7,240,145 ("Holman"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • U.S. Patent No. 7,155,627 ("Matsui '627"); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • U.S. Patent No. 7,092,299 ("Kwak"); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen '578"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent Application Publication No.

	2003/0133331 ("LaBerge '331"); • U.S. Patent Publication. No. 2002/0188816 ("Johnson '816"); • U.S. Patent Application Publication No. 2004/0034755 ("LaBerge '755"); • U.S. Patent Application Publication No. 2005/0050255 ("Jeddeloh"); • U.S. Patent No. 6,446,184 ("Dell '184"); • U.S. Patent Application Publication No. 2005/0257109 ("Averbuj"); • U.S. Patent No. 6,820,163 ("McCall"); • U.S. Patent No. 6,564,287 ("Lee '287"); • U.S. Patent No. 7,222,224 ("Woo"); • U.S. Patent No. 7,334,150 ("Ruckerbauer"); • U.S. Patent No. 7,289,383 ("Cornelius"); • U.S. Patent No. 6,392,909 ("Jang"); • U.S. Patent No. 6,529,423 ("Yoon"); • U.S. Patent No. 6,262,938 ("Lee '938"); • U.S. Patent No. 7,206,896 ("Perego '896"); • U.S. Patent No. 6,205,062 ("Kim '062"); • U.S. Patent No. 7,043,617 ("Williams '617"); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 7,433,258 ("Rao"); • U.S. Pat. No. 5,581,498 ("Ludwig"); • U.S. Patent No. 5,926,827 ("Dell '827"); • U.S. Patent Application Publication No. US 2006/0195631 ("Rajamani"); • U.S. Patent Application Publication No. 2005/0198449 ("Haskell"); • and/or • The knowledge of a person of ordinary skill in the art.
Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Datasheet	• The '215 Patent's Admitted Prior Art ("APA"); • U.S. Patent Application Publication No. 2003/0204688 ("Lee '688"); • DDR3 Functional Outlook; • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2003/0145156 ("Khandekar"); • U.S. Patent No. 6,862,653 ("Dodd");

	• U.S. Patent Application Publication No. 2003/0117864 (“Hampel”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • JEDEC Standards; • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • Kentron’s Quad Band Memory System (“QBM”); • U.S. Patent No. 7,206,896 (“Perego ’896”) • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent No. 6,262,938 (“Lee ’938”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 6,205,062 ("Kim ’062"); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen ’578"); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 7,024,518 (“Halbert ’518”) • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”);

	• U.S. Patent No. 7,366,827 (Lee ’827); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); and/or • The knowledge of a person of ordinary skill in the art.
Micron DDR SDRAM RDIMM, MT36VDDF12872 and/or MT36VDDF25672 Products	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • DDR3 Functional Outlook; • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • U.S. Patent No. 6,862,653 (“Dodd”); • U.S. Patent Application Publication No. 2003/0117864 (“Hampel”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • JEDEC Standards; • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • Kentron’s Quad Band Memory System (“QBM”); • U.S. Patent No. 7,206,896 (“Perego ’896”) • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent No. 6,262,938 (“Lee ’938”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 6,205,062 ("Kim ’062"); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”);

	• U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen ’578"); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 7,024,518 (“Halbert ’518”) • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 7,366,827 (Lee ’827); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); and/or • The knowledge of a person of ordinary skill in the art.

As mentioned above, Defendants have not yet completed their search or discovery concerning additional prior art. Moreover, the exemplary combinations are provided based on Defendants’ current understanding of the Asserted Claims and Plaintiff’s apparent view of the scope of those claims as shown, for example, in Plaintiff’s Infringement Contentions. Further, a *Markman* Order has not yet been issued in this case. As such, Defendants’ inclusion of exemplary combinations does not preclude them from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

3. U.S. Patent No. 11,093,417

Pursuant to P.R. 3-3(a) and (b), Defendants identify in Appendix C the prior art references that render obvious the Asserted Claims of the ’417 patent and include below exemplary

in expert reports regarding invalidity.

For at least the reasons described above, it would have been obvious to one of ordinary skill in the art to combine each prior art reference listed in Appendix C with any other reference or references listed in Appendix C along with the knowledge of one of ordinary skill in the art to arrive at the inventions claimed in the '417 patent. For example, and without limitation, the Asserted Claims of the '417 patent would have been obvious to one of ordinary skill in the art in view of the following combinations:

Patent No. or Title (Primary Inventor/Author)	**In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))**
The '417 Patent's Admitted Prior Art ("APA")	• U.S. Patent No. 7,103,742 ("Mailloux"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • U.S. Patent No. 6,851,032 ("LaBerge '032") ; • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent No. 7,024,518 ("Halbert '518"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); • FBDIMM Architecture & Protocol; • Kentron's Quad Band Memory System ("QBM"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • DDR3 Functional Outlook; • U.S. Patent No. 6,154,821 ("Barth"); • U.S. Patent No. 6,226,755 ("Reeves"); • U.S. Patent No. 6,742,098 ("Halbert '098"); • U.S. Patent No. 6,940,782 ("Matsui '782"); • U.S. Patent No. 7,196,948 ("Vemula"); • U.S. Patent Application Publication No. 2002/0133666 ("Janzen '666"); • U.S. Patent Application Publication No. 2004/0103258 ("Blockmon"); • U.S. Patent Application Publication No.

	2004/0260864 (“Lee ’864”); • U.S. Patent Application Publication No. 2005/0044304 (“James”); • International Patent Application Publication No. WO 96/020446 (“Williams ’446”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen ’578"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • International Patent Application Publication No. WO 01/037090 (“Wong ’090”); and/or

	• The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 7,103,742 ("Mailloux")	• The '417 Patent's Admitted Prior Art ("APA"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); • U.S. Patent No. 6,851,032 ("LaBerge '032") ; • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent No. 7,024,518 ("Halbert '518"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • U.S. Patent No. 6,742,098 ("Halbert '098"); • U.S. Patent Application Publication No. 2004/0103258 ("Blockmon"); • International Patent Application Publication No. WO 96/020446 ("Williams '446"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 ("Dell '184"); • U.S. Patent No. 6,205,062 ("Kim '062"); • JEDEC Standards; • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent Application Publication No. 2004/0260864 ("Lee '864"); • International Patent Application Publication No. WO 01/037090 ("Wong '090"); • U.S. Patent No. 6,154,821 ("Barth"); • U.S. Patent No. 6,226,755 ("Reeves"); • U.S. Patent No. 6,940,782 ("Matsui '782"); • U.S. Patent No. 7,196,948 ("Vemula"); • U.S. Patent Application Publication No. 2002/0133666 ("Janzen '666"); • U.S. Patent Application Publication No. 2003/0204688 ("Lee '688"); • U.S. Patent No. 7,240,145 ("Holman"); • U.S. Patent No. 7,092,299 ("Kwak");

	• U.S. Patent Application Publication No. 2002/0118578 ("Janzen '578"); • U.S. Patent No. 7,149,841 ("LaBerge '841"); • U.S. Patent No. 7,366,827 ("Lee '827"); • U.S. Patent No. 7,043,617 ("Williams '617"); • U.S. Patent No. 7,433,258 ("Rao"); • U.S. Pat. No. 5,581,498 ("Ludwig"); • U.S. Patent No. 5,926,827 ("Dell '827"); • U.S. Patent Application Publication No. US 2006/0195631 ("Rajamani"); • U.S. Patent Application Publication No. 2005/0198449 ("Haskell"); • U.S. Patent Application Publication No. 2005/0257109 ("Averbuj"); • FBDIMM Architecture & Protocol; • U.S. Patent No. 7,155,627 ("Matsui '627"); • U.S. Patent No. 7,222,224 ("Woo"); • U.S. Patent No. 7,289,383 ("Cornelius"); • U.S. Patent No. 6,529,423 ("Yoon"); • U.S. Patent No. 7,206,896 ("Perego '896"); • U.S. Patent No. 7,212,424 ("Johnson '424"); • U.S. Patent No. 5,712,811 ("Kim '811"); • U.S. Patent No. 7,334,150 ("Ruckerbauer"); • Kentron's Quad Band Memory System ("QBM"); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent Application Publication No. 2006/0117152 ("Amidi")	• The '417 Patent's Admitted Prior Art ("APA"); • U.S. Patent No. 7,103,742 ("Mailloux"); • U.S. Patent No. 6,851,032 ("LaBerge '032") ; • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent No. 7,024,518 ("Halbert '518"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A");

	• U.S. Patent No. 6,742,098 (“Halbert ’098”); • U.S. Patent Application Publication No. 2004/0103258 (“Blockmon”); • International Patent Application Publication No. WO 96/020446 (“Williams ’446”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • JEDEC Standards; • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent Application Publication No. 2004/0260864 (“Lee ’864”); • International Patent Application Publication No. WO 01/037090 (“Wong ’090”); • U.S. Patent No. 6,154,821 (“Barth”); • U.S. Patent No. 6,226,755 (“Reeves”); • U.S. Patent No. 6,940,782 (“Matsui ’782”); • U.S. Patent No. 7,196,948 (“Vemula”); • U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen ’578"); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”);

	• U.S. Patent No. 7,222,224 ("Woo"); • U.S. Patent No. 7,289,383 ("Cornelius"); • U.S. Patent No. 6,529,423 ("Yoon"); • U.S. Patent No. 7,206,896 ("Perego '896"); • U.S. Patent No. 7,212,424 ("Johnson '424"); • U.S. Patent No. 5,712,811 ("Kim '811"); • U.S. Patent No. 7,334,150 ("Ruckerbauer"); • Kentron's Quad Band Memory System ("QBM"); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art of a person of ordinary skill in the art.
U.S. Patent No. 6,851,032 ("LaBerge '032")	• The '417 Patent's Admitted Prior Art ("APA"); • U.S. Patent No. 7,103,742 ("Mailloux"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent No. 7,024,518 ("Halbert '518"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • U.S. Patent No. 6,742,098 ("Halbert '098"); • U.S. Patent Application Publication No. 2004/0103258 ("Blockmon"); • International Patent Application Publication No. WO 96/020446 ("Williams '446"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 ("Dell '184"); • U.S. Patent No. 6,205,062 ("Kim '062"); • JEDEC Standards; • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent Application Publication No. 2004/0260864 ("Lee '864"); • International Patent Application Publication No.

	WO 01/037090 (“Wong ’090”); • U.S. Patent No. 6,154,821 (“Barth”); • U.S. Patent No. 6,226,755 (“Reeves”); • U.S. Patent No. 6,940,782 (“Matsui ’782”); • U.S. Patent No. 7,196,948 (“Vemula”); • U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen ’578"); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 7,155,627 (“Matsui ’627”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • Kentron’s Quad Band Memory System (“QBM”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in

	the art.
U.S. Patent No. 7,363,422 ("Perego '422")	• The '417 Patent's Admitted Prior Art ("APA"); • U.S. Patent No. 7,103,742 ("Mailloux"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • U.S. Patent No. 6,851,032 ("LaBerge '032") ; • U.S. Patent No. 7,024,518 ("Halbert '518"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • U.S. Patent No. 6,742,098 ("Halbert '098"); • U.S. Patent Application Publication No. 2004/0103258 ("Blockmon"); • International Patent Application Publication No. WO 96/020446 ("Williams '446"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 ("Dell '184"); • U.S. Patent No. 6,205,062 ("Kim '062"); • JEDEC Standards; • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent Application Publication No. 2004/0260864 ("Lee '864"); • International Patent Application Publication No. WO 01/037090 ("Wong '090"); • U.S. Patent No. 6,154,821 ("Barth"); • U.S. Patent No. 6,226,755 ("Reeves"); • U.S. Patent No. 6,940,782 ("Matsui '782"); • U.S. Patent No. 7,196,948 ("Vemula"); • U.S. Patent Application Publication No. 2002/0133666 ("Janzen '666"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); • U.S. Patent Application Publication No. 2003/0204688 ("Lee '688"); • U.S. Patent No. 7,240,145 ("Holman"); • U.S. Patent No. 7,092,299 ("Kwak"); • U.S. Patent Application Publication No.

	2002/0118578 ("Janzen '578"); • U.S. Patent No. 7,149,841 ("LaBerge '841"); • U.S. Patent No. 7,366,827 ("Lee '827"); • U.S. Patent No. 7,043,617 ("Williams '617"); • U.S. Patent No. 7,433,258 ("Rao"); • U.S. Pat. No. 5,581,498 ("Ludwig"); • U.S. Patent No. 5,926,827 ("Dell '827"); • U.S. Patent Application Publication No. US 2006/0195631 ("Rajamani"); • U.S. Patent Application Publication No. 2005/0198449 ("Haskell"); • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2005/0257109 ("Averbuj"); • U.S. Patent No. 7,222,224 ("Woo"); • U.S. Patent No. 7,289,383 ("Cornelius"); • U.S. Patent No. 6,529,423 ("Yoon"); • U.S. Patent No. 7,206,896 ("Perego '896"); • U.S. Patent No. 7,212,424 ("Johnson '424"); • U.S. Patent No. 5,712,811 ("Kim '811"); • U.S. Patent No. 7,334,150 ("Ruckerbauer"); • Kentron's Quad Band Memory System ("QBM"); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 7,024,518 ("Halbert '518")	• The '417 Patent's Admitted Prior Art ("APA"); • U.S. Patent No. 7,103,742 ("Mailloux"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • U.S. Patent No. 6,851,032 ("LaBerge '032") ; • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein");

	• U.S. Patent No. 6,742,098 ("Halbert '098"); • U.S. Patent Application Publication No. 2004/0103258 ("Blockmon"); • International Patent Application Publication No. WO 96/020446 ("Williams '446"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 ("Dell '184"); • U.S. Patent No. 6,205,062 ("Kim '062"); • JEDEC Standards; • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent Application Publication No. 2004/0260864 ("Lee '864"); • International Patent Application Publication No. WO 01/037090 ("Wong '090"); • FBDIMM Architecture & Protocol; • U.S. Patent No. 6,154,821 ("Barth"); • U.S. Patent No. 6,226,755 ("Reeves"); • U.S. Patent No. 6,940,782 ("Matsui '782"); • U.S. Patent No. 7,196,948 ("Vemula"); • U.S. Patent Application Publication No. 2002/0133666 ("Janzen '666"); • U.S. Patent Application Publication No. 2003/0204688 ("Lee '688"); • U.S. Patent No. 7,240,145 ("Holman"); • U.S. Patent No. 7,092,299 ("Kwak"); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen '578"); • U.S. Patent No. 7,149,841 ("LaBerge '841"); • U.S. Patent No. 7,366,827 ("Lee '827"); • U.S. Patent No. 7,043,617 ("Williams '617"); • U.S. Patent No. 7,433,258 ("Rao"); • U.S. Pat. No. 5,581,498 ("Ludwig"); • U.S. Patent No. 5,926,827 ("Dell '827"); • U.S. Patent Application Publication No. US 2006/0195631 ("Rajamani"); • U.S. Patent Application Publication No. 2005/0198449 ("Haskell"); • U.S. Patent Application Publication No. 2005/0257109 ("Averbuj"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent No. 7,222,224 ("Woo");

	• U.S. Patent No. 7,289,383 ("Cornelius"); • U.S. Patent No. 6,529,423 ("Yoon"); • U.S. Patent No. 7,206,896 ("Perego '896"); • U.S. Patent No. 7,212,424 ("Johnson '424"); • U.S. Patent No. 5,712,811 ("Kim '811"); • U.S. Patent No. 7,334,150 ("Ruckerbauer"); • Kentron's Quad Band Memory System ("QBM"); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry")	• The '417 Patent's Admitted Prior Art ("APA"); • U.S. Patent No. 7,103,742 ("Mailloux"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent No. 6,851,032 ("LaBerge '032") ; • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent No. 7,024,518 ("Halbert '518"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • U.S. Patent No. 6,742,098 ("Halbert '098"); • U.S. Patent Application Publication No. 2004/0103258 ("Blockmon"); • International Patent Application Publication No. WO 96/020446 ("Williams '446"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 ("Dell '184"); • U.S. Patent No. 6,205,062 ("Kim '062"); • JEDEC Standards; • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2004/0260864 ("Lee '864"); • International Patent Application Publication No.

	WO 01/037090 (“Wong ’090”); • U.S. Patent No. 6,154,821 (“Barth”); • U.S. Patent No. 6,226,755 (“Reeves”); • U.S. Patent No. 6,940,782 (“Matsui ’782”); • U.S. Patent No. 7,196,948 (“Vemula”); • U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen ’578"); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • FBDIMM Architecture & Protocol; • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • Kentron’s Quad Band Memory System (“QBM”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 6,493,250 (“Halbert ’250”)	• The ’417 Patent’s Admitted Prior Art (“APA”); • U.S. Patent No. 7,103,742 (“Mailloux”); • U.S. Patent Application Publication No.

	2006/0117152 (“Amidi”); • U.S. Patent No. 6,851,032 (“LaBerge ’032”) ; • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent No. 6,742,098 (“Halbert ’098”); • U.S. Patent Application Publication No. 2004/0103258 (“Blockmon”); • International Patent Application Publication No. WO 96/020446 (“Williams ’446”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • JEDEC Standards; • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2004/0260864 (“Lee ’864”); • International Patent Application Publication No. WO 01/037090 (“Wong ’090”); • U.S. Patent No. 6,154,821 (“Barth”); • U.S. Patent No. 6,226,755 (“Reeves”); • U.S. Patent No. 6,940,782 (“Matsui ’782”); • U.S. Patent No. 7,196,948 (“Vemula”); • U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen ’578"); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US

	2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • FBDIMM Architecture & Protocol; • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • Kentron’s Quad Band Memory System (“QBM”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent Application Publication No. 2001/0008006 (“Klein”)	• The ’417 Patent’s Admitted Prior Art (“APA”); • U.S. Patent No. 7,103,742 (“Mailloux”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 6,851,032 (“LaBerge ’032”) ; • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent No. 6,742,098 (“Halbert ’098”); • U.S. Patent Application Publication No. 2004/0103258 (“Blockmon”); • International Patent Application Publication No. WO 96/020446 (“Williams ’446”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob);

	• U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • JEDEC Standards; • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2004/0260864 (“Lee ’864”); • International Patent Application Publication No. WO 01/037090 (“Wong ’090”); • U.S. Patent No. 6,154,821 (“Barth”); • U.S. Patent No. 6,226,755 (“Reeves”); • U.S. Patent No. 6,940,782 (“Matsui ’782”); • U.S. Patent No. 7,196,948 (“Vemula”); • U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen ’578"); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • FBDIMM Architecture & Protocol; • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • Kentron’s Quad Band Memory System (“QBM”);

	• Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
JEDEC Standards	• The '417 Patent's Admitted Prior Art ("APA"); • U.S. Patent No. 7,103,742 ("Mailloux"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent No. 6,851,032 ("LaBerge '032") ; • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent No. 7,024,518 ("Halbert '518"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • U.S. Patent No. 6,742,098 ("Halbert '098"); • U.S. Patent Application Publication No. 2004/0103258 ("Blockmon"); • International Patent Application Publication No. WO 96/020446 ("Williams '446"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 ("Dell '184"); • U.S. Patent No. 6,205,062 ("Kim '062"); • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent Application Publication No. 2004/0260864 ("Lee '864"); • International Patent Application Publication No. WO 01/037090 ("Wong '090"); • U.S. Patent No. 6,154,821 ("Barth"); • U.S. Patent No. 6,226,755 ("Reeves"); • U.S. Patent No. 6,940,782 ("Matsui '782"); • U.S. Patent No. 7,196,948 ("Vemula"); • U.S. Patent Application Publication No. 2002/0133666 ("Janzen '666");

	• U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen ’578"); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • FBDIMM Architecture & Protocol; • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • Kentron’s Quad Band Memory System (“QBM”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”)	• The ’417 Patent’s Admitted Prior Art (“APA”); • U.S. Patent No. 7,103,742 (“Mailloux”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 6,851,032 (“LaBerge ’032”) ; • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent No. 7,024,518 (“Halbert ’518”);

	• DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • U.S. Patent No. 6,742,098 ("Halbert '098"); • U.S. Patent Application Publication No. 2004/0103258 ("Blockmon"); • International Patent Application Publication No. WO 96/020446 ("Williams '446"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 ("Dell '184"); • U.S. Patent No. 6,205,062 ("Kim '062"); • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent Application Publication No. 2004/0260864 ("Lee '864"); • International Patent Application Publication No. WO 01/037090 ("Wong '090"); • U.S. Patent No. 6,154,821 ("Barth"); • U.S. Patent No. 6,226,755 ("Reeves"); • U.S. Patent No. 6,940,782 ("Matsui '782"); • U.S. Patent No. 7,196,948 ("Vemula"); • U.S. Patent Application Publication No. 2002/0133666 ("Janzen '666"); • U.S. Patent Application Publication No. 2003/0204688 ("Lee '688"); • U.S. Patent No. 7,240,145 ("Holman"); • U.S. Patent No. 7,092,299 ("Kwak"); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen '578"); • U.S. Patent No. 7,149,841 ("LaBerge '841"); • U.S. Patent No. 7,366,827 ("Lee '827"); • U.S. Patent No. 7,043,617 ("Williams '617"); • U.S. Patent No. 7,433,258 ("Rao"); • U.S. Pat. No. 5,581,498 ("Ludwig"); • U.S. Patent No. 5,926,827 ("Dell '827"); • U.S. Patent Application Publication No. US 2006/0195631 ("Rajamani"); • U.S. Patent Application Publication No. 2005/0198449 ("Haskell"); • U.S. Patent Application Publication No. 2005/0257109 ("Averbuj"); • FBDIMM Architecture & Protocol;

	• U.S. Patent No. 7,222,224 ("Woo"); • U.S. Patent No. 7,289,383 ("Cornelius"); • U.S. Patent No. 6,529,423 ("Yoon"); • U.S. Patent No. 7,206,896 ("Perego '896"); • U.S. Patent No. 7,212,424 ("Johnson '424"); • U.S. Patent No. 5,712,811 ("Kim '811"); • U.S. Patent No. 7,334,150 ("Ruckerbauer"); • Kentron's Quad Band Memory System ("QBM"); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119")	• The '417 Patent's Admitted Prior Art ("APA"); • U.S. Patent No. 7,103,742 ("Mailloux"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent No. 6,851,032 ("LaBerge '032") ; • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent No. 7,024,518 ("Halbert '518"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • U.S. Patent No. 6,742,098 ("Halbert '098"); • U.S. Patent Application Publication No. 2004/0103258 ("Blockmon"); • International Patent Application Publication No. WO 96/020446 ("Williams '446"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 ("Dell '184"); • U.S. Patent No. 6,205,062 ("Kim '062"); • JEDEC Standards; • FBDIMM Architecture & Protocol;

	• U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent Application Publication No. 2004/0260864 (“Lee ’864”); • International Patent Application Publication No. WO 01/037090 (“Wong ’090”); • U.S. Patent No. 6,154,821 (“Barth”); • U.S. Patent No. 6,226,755 (“Reeves”); • U.S. Patent No. 6,940,782 (“Matsui ’782”); • U.S. Patent No. 7,196,948 (“Vemula”); • U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen ’578"); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • FBDIMM Architecture & Protocol; • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • Kentron’s Quad Band Memory System (“QBM”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or

	• The knowledge of a person of ordinary skill in the art.
DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C")	• The '417 Patent's Admitted Prior Art ("APA"); • U.S. Patent No. 7,103,742 ("Mailloux"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent No. 6,851,032 ("LaBerge '032") ; • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent No. 7,024,518 ("Halbert '518"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); • U.S. Patent No. 6,742,098 ("Halbert '098"); • U.S. Patent Application Publication No. 2004/0103258 ("Blockmon"); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • International Patent Application Publication No. WO 96/020446 ("Williams '446"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 ("Dell '184"); • U.S. Patent No. 6,205,062 ("Kim '062"); • JEDEC Standards; • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent Application Publication No. 2004/0260864 ("Lee '864"); • International Patent Application Publication No. WO 01/037090 ("Wong '090"); • U.S. Patent No. 6,154,821 ("Barth"); • U.S. Patent No. 6,226,755 ("Reeves"); • U.S. Patent No. 6,940,782 ("Matsui '782"); • U.S. Patent No. 7,196,948 ("Vemula"); • U.S. Patent Application Publication No. 2002/0133666 ("Janzen '666"); • U.S. Patent Application Publication No. 2003/0204688 ("Lee '688"); • U.S. Patent No. 7,240,145 ("Holman"); • U.S. Patent No. 7,092,299 ("Kwak"); • U.S. Patent Application Publication No.

	2002/0118578 ("Janzen '578"); • U.S. Patent No. 7,149,841 ("LaBerge '841"); • U.S. Patent No. 7,366,827 ("Lee '827"); • U.S. Patent No. 7,043,617 ("Williams '617"); • U.S. Patent No. 7,433,258 ("Rao"); • U.S. Pat. No. 5,581,498 ("Ludwig"); • U.S. Patent No. 5,926,827 ("Dell '827"); • U.S. Patent Application Publication No. US 2006/0195631 ("Rajamani"); • U.S. Patent Application Publication No. 2005/0198449 ("Haskell"); • U.S. Patent Application Publication No. 2005/0257109 ("Averbuj"); • FBDIMM Architecture & Protocol; • U.S. Patent No. 7,222,224 ("Woo"); • U.S. Patent No. 7,289,383 ("Cornelius"); • U.S. Patent No. 6,529,423 ("Yoon"); • U.S. Patent No. 7,206,896 ("Perego '896"); • U.S. Patent No. 7,212,424 ("Johnson '424"); • U.S. Patent No. 5,712,811 ("Kim '811"); • U.S. Patent No. 7,334,150 ("Ruckerbauer"); • Kentron's Quad Band Memory System ("QBM"); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
Kentron's Quad Band Memory System ("QBM")	• The '417 Patent's Admitted Prior Art ("APA"); • U.S. Patent No. 7,103,742 ("Mailloux"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent No. 6,851,032 ("LaBerge '032") ; • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent No. 7,024,518 ("Halbert '518"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • DDR SDRAM RDIMM Design Specification

	JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • U.S. Patent No. 6,742,098 ("Halbert '098"); • U.S. Patent Application Publication No. 2004/0103258 ("Blockmon"); • International Patent Application Publication No. WO 96/020446 ("Williams '446"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 ("Dell '184"); • U.S. Patent No. 6,205,062 ("Kim '062"); • JEDEC Standards; • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent Application Publication No. 2004/0260864 ("Lee '864"); • International Patent Application Publication No. WO 01/037090 ("Wong '090"); • U.S. Patent No. 6,154,821 ("Barth"); • U.S. Patent No. 6,226,755 ("Reeves"); • U.S. Patent No. 6,940,782 ("Matsui '782"); • U.S. Patent No. 7,196,948 ("Vemula"); • U.S. Patent Application Publication No. 2002/0133666 ("Janzen '666"); • U.S. Patent Application Publication No. 2003/0204688 ("Lee '688"); • U.S. Patent No. 7,240,145 ("Holman"); • U.S. Patent No. 7,092,299 ("Kwak"); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen '578"); • U.S. Patent No. 7,149,841 ("LaBerge '841"); • U.S. Patent No. 7,366,827 ("Lee '827"); • U.S. Patent No. 7,043,617 ("Williams '617"); • U.S. Patent No. 7,433,258 ("Rao"); • U.S. Pat. No. 5,581,498 ("Ludwig"); • U.S. Patent No. 5,926,827 ("Dell '827"); • U.S. Patent Application Publication No. US 2006/0195631 ("Rajamani"); • U.S. Patent Application Publication No. 2005/0198449 ("Haskell"); • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2005/0257109 ("Averbuj"); • U.S. Patent No. 7,222,224 ("Woo");

	• U.S. Patent No. 7,289,383 ("Cornelius"); • U.S. Patent No. 6,529,423 ("Yoon"); • U.S. Patent No. 7,206,896 ("Perego '896"); • U.S. Patent No. 7,212,424 ("Johnson '424"); • U.S. Patent No. 5,712,811 ("Kim '811"); • U.S. Patent No. 7,334,150 ("Ruckerbauer"); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
DDR3 Functional Outlook	• The '417 Patent's Admitted Prior Art ("APA"); • U.S. Patent No. 7,103,742 ("Mailloux"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • U.S. Patent No. 6,851,032 ("LaBerge '032") ; • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent No. 7,024,518 ("Halbert '518"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • U.S. Patent No. 7,155,627 ("Matsui '627"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • U.S. Patent Application Publication No. 2021/0149829 ("Lee '829"); • U.S. Patent No. 6,742,098 ("Halbert '098"); • U.S. Patent Application Publication No. 2004/0103258 ("Blockmon"); • International Patent Application Publication No. WO 96/020446 ("Williams '446"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 ("Dell '184"); • U.S. Patent No. 6,205,062 ("Kim '062"); • JEDEC Standards; • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent Application Publication No.

	2004/0260864 (“Lee ’864”); • International Patent Application Publication No. WO 01/037090 (“Wong ’090”); • U.S. Patent No. 6,154,821 (“Barth”); • U.S. Patent No. 6,226,755 (“Reeves”); • U.S. Patent No. 6,940,782 (“Matsui ’782”); • U.S. Patent No. 7,196,948 (“Vemula”); • U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen ’578"); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • FBDIMM Architecture & Protocol; • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent Application Publication No. 2021/0149829 (“Lee ‘829”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • Kentron’s Quad Band Memory System (“QBM”); and/or

	• The knowledge of a person of ordinary skill in the art.
FBDIMM Architecture & Protocol	• The '417 Patent's Admitted Prior Art ("APA"); • U.S. Patent No. 7,103,742 ("Mailloux"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • U.S. Patent No. 6,851,032 ("LaBerge '032"); • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent No. 7,024,518 ("Halbert '518"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • U.S. Patent No. 6,742,098 ("Halbert '098"); • U.S. Patent Application Publication No. 2004/0103258 ("Blockmon"); • International Patent Application Publication No. WO 96/020446 ("Williams '446"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • U.S. Patent No. 6,446,184 ("Dell '184"); • U.S. Patent No. 6,205,062 ("Kim '062"); • JEDEC Standards; • Kentron's Quad Band Memory System ("QBM"); • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent Application Publication No. 2004/0260864 ("Lee '864"); • International Patent Application Publication No. WO 01/037090 ("Wong '090"); • U.S. Patent No. 6,154,821 ("Barth"); • U.S. Patent No. 6,226,755 ("Reeves"); • U.S. Patent No. 6,940,782 ("Matsui '782"); • U.S. Patent No. 7,196,948 ("Vemula"); • U.S. Patent Application Publication No. 2002/0133666 ("Janzen '666"); • U.S. Patent Application Publication No. 2003/0204688 ("Lee '688"); • U.S. Patent No. 7,240,145 ("Holman");

	• U.S. Patent No. 7,092,299 ("Kwak"); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen '578"); • U.S. Patent No. 7,149,841 ("LaBerge '841"); • U.S. Patent No. 7,366,827 ("Lee '827"); • U.S. Patent No. 7,043,617 ("Williams '617"); • U.S. Patent No. 7,433,258 ("Rao"); • U.S. Pat. No. 5,581,498 ("Ludwig"); • U.S. Patent No. 5,926,827 ("Dell '827"); • U.S. Patent Application Publication No. US 2006/0195631 ("Rajamani"); • U.S. Patent Application Publication No. 2005/0198449 ("Haskell"); • U.S. Patent Application Publication No. 2005/0257109 ("Averbuj"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); • U.S. Patent Application Publication No. 2021/0149829 ("Lee '829"); • U.S. Patent No. 7,222,224 ("Woo"); • U.S. Patent No. 7,289,383 ("Cornelius"); • U.S. Patent No. 6,529,423 ("Yoon"); • U.S. Patent No. 7,206,896 ("Perego '896"); • U.S. Patent No. 7,212,424 ("Johnson '424"); • U.S. Patent No. 5,712,811 ("Kim '811"); • U.S. Patent No. 7,334,150 ("Ruckerbauer"); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Datasheet	• The '417 Patent's Admitted Prior Art ("APA"); • U.S. Patent No. 7,103,742 ("Mailloux"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent No. 6,851,032 ("LaBerge '032") ; • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent No. 7,024,518 ("Halbert '518");

	• U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • Kentron’s Quad Band Memory System (“QBM”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • U.S. Patent No. 6,742,098 (“Halbert ’098”); • U.S. Patent Application Publication No. 2004/0103258 (“Blockmon”); • International Patent Application Publication No. WO 96/020446 (“Williams ’446”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • JEDEC Standards; • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent Application Publication No. 2004/0260864 (“Lee ’864”); • International Patent Application Publication No. WO 01/037090 (“Wong ’090”); • U.S. Patent No. 6,154,821 (“Barth”); • U.S. Patent No. 6,226,755 (“Reeves”); • U.S. Patent No. 6,940,782 (“Matsui ’782”); • U.S. Patent No. 7,196,948 (“Vemula”); • U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen ’578"); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • Kentron’s Quad Band Memory System (“QBM”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US

	2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
Micron DDR SDRAM RDIMM, MT36VDDF12872 and/or MT36VDDF25672 Products	• The ’417 Patent’s Admitted Prior Art (“APA”); • U.S. Patent No. 7,103,742 (“Mailloux”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 6,851,032 (“LaBerge ’032”) ; • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • U.S. Patent No. 6,742,098 (“Halbert ’098”); • U.S. Patent Application Publication No. 2004/0103258 (“Blockmon”); • International Patent Application Publication No. WO 96/020446 (“Williams ’446”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • JEDEC Standards;

	• U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent Application Publication No. 2004/0260864 (“Lee ’864”); • International Patent Application Publication No. WO 01/037090 (“Wong ’090”); • U.S. Patent No. 6,154,821 (“Barth”); • U.S. Patent No. 6,226,755 (“Reeves”); • U.S. Patent No. 6,940,782 (“Matsui ’782”); • U.S. Patent No. 7,196,948 (“Vemula”); • U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 ("Janzen ’578"); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.

As mentioned above, Defendants have not yet completed their search or discovery

text referring to a figure include the figure and caption as well. Portions relevant to dependent claims incorporate by reference the citations to the chain of claims from which that dependent claim derives. Likewise, portions related to subsequent limitations that refer to claim elements identified, described, and/or cited to in earlier limitations may rely on the citations related to those portions of the claim chart that identify and/or describe these elements.

Throughout the invalidity claim charts in Appendices A-C, Defendants provide examples of where references disclose subject matter recited in preambles of the Asserted Claims, regardless whether the preambles limit the claims. Defendants reserve the right to argue that the preambles are or are not limitations. Further, where an entry in a claim chart corresponding to a given limitation refers back to the discussion of another claim, the entry incorporates all evidence cited for the other claim.

VI. P. R. 3-3(d) – Other Grounds for Invalidity

A. U.S. Patent No. 7,619,912

Pursuant to Rule 3-3(d), Defendants hereby identify grounds of invalidity for the ’912 Patent based on lack of written description under 35 U.S.C. § 112, first paragraph; lack of enablement under 35 U.S.C. § 112, first paragraph; indefiniteness under 35 U.S.C. § 112, second paragraph; and indefiniteness under 35 U.S.C. § 112, sixth paragraph. These contentions shall not be construed as an admission that any claim construction advanced by Defendants in this case is in any way inconsistent, flawed, or erroneous. Nor should these contentions prevent Defendants from advancing claim construction and/or non-infringement positions in lieu of, or in addition to, invalidity positions. Further, these contentions shall not be construed as an admission of or acquiescence to Plaintiff’s purported construction of the claim language or of other positions advanced by Plaintiff during the course of this litigation. Defendants’ invalidity contentions under

35 U.S.C. § 112 may depend, in part, on the Court's claim construction, as well as Plaintiff's alleged scope of the '912 patent Asserted Claims. Consequently, Defendants only identify the issues under 35 U.S.C. § 112 of which they are presently aware.

1. Lack of Written Description and/or Enablement Under 35 U.S.C. § 112, ¶ 1

The '912 Patent does not provide sufficient written description to establish that the inventors were in possession of the alleged inventions recited in the '912 patent Asserted Claims at the time the '912 patent was filed. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010). In other words, the applicants did not describe their purported inventions in a manner that "reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *Id*. One of ordinary skill in the art would not have understood that the inventors were in possession of the full scope of the claimed apparatus and methods.

The specification of the '912 patent also '912 not enable one of ordinary skill in the art to make and/or use certain recited elements of the '912 patent Asserted Claims without undue experimentation. To the extent the following limitations are definite (under 35 U.S.C. § 112, ¶ 2), the application that became the '912 patent fails to sufficiently describe or enable them as required by 35 U.S.C. § 112, ¶ 1:[5]

Term	Relevant Claim(s)
"rank"	1, 15, 16, 28, 39, 77, 80, 82, 86, 88, 90
"logic element"	1, 6, 8, 15, 16, 24, 27, 28, 29, 39, 43, 45, 59, 60, 77, 80, 82, 86, 88, 90

[5] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

Term	Relevant Claim(s)
"buffer"	1, 15, 28, 39, 77 80, 82, 86, 88, 90
"in the direction along the first side"	11, 47
"in the direction along the second side"	11, 47
"register"	1, 8, 15, 16, 27, 28, 39, 45, 58, 72, 77, 80, 82, 86, 88, 90
"receiving a set of input [control] signals from the computer system, the set of input [control] signals comprising at least one row/column address signal, bank address signals, [and at least one/a] chip-select signal[, and an input command signal]"	1, 15, 16, 28, 77, 80, 82, 86, 88
"the set of input control signals corresponding to a second number of DDR memory devices"	1, 77, 80, 82
"generating a [set/plurality] of output [control] signals in response to the [set/plurality of input [control] signals"	1, 15, 16, 28, 39, 77, 80, 82, 86, 88, 90
"the set of output control signals corresponding to the first number of DDR memory devices"	1, 77, 80, 82
"responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices"	1, 77, 80, 82
"the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks"	1, 77, 80, 82
"the phase-lock loop device operatively coupled to the plurality of DDR [memory/DRAM] devices, the logic element, and the register"	1, 15, 16, 28, 77, 80, 82, 86, 88
"in respons[e/ive] to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR [DRAM] memory devices, the logic element, and the register"	1, 15, 28, 39, 77, 82, 86, 88, 90
"the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals"	1, 15, 28, 77, 82, 86, 88
"transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices"	1, 77, 82
"the [at least one] row/column address signal received by the logic element comprises [at least one/a] row address signal received by the logic element"	1, 15, 28, 39, 77, 80, 82, 86, 90
"the plurality of row[/column] address signals received by the register are separate from the [at least one] row address signal received by the logic element"	1, 15, 28, 39, 77, 80, 82, 86, 90

Term	Relevant Claim(s)
"generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response to at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the [set/plurality] of input [control] signals and (iv) the PLL clock signal."	1, 15, 28, 39
"wherein the set of input control signals comprises a first number of chip-select signals and wherein the set of output control signals comprises a second number of chip-select signals"	3
"custom-designed semiconductor device"	6, 24, 29, 41
"spaced from"	10, 11, 46, 47
"a direction along the [first/second] side"	11, 47
"the set of input signals configured to control a second number of DDR [memory/DRAM] devices"	15, 16, 28, 86, 88
"the set of output signals configured to control the first number of DDR [memory/DRAM] devices"	15, 16, 28, 86, 88
"the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks"	15, 16, 86
"transmits the buffered plurality of row/column address signals and the buffered bank address signals to the at least one DDR [memory/DRAM] device of the selected one or two ranks of the first number of ranks"	15, 28, 86, 88
"the command signal is transmitted to only one DDR memory device at a time"	16
"the command signal is transmitted to two ranks of the first number of ranks at a time"	18
"the command signal is transmitted to the two ranks of the first number of ranks concurrently"	20
"the set of input signals comprises a density bit which is a row address bit"	22
"the circuit is configured to store the row address bit during an activate command for a selected bank"	22
"double-data-rate (DDR) dynamic random access memory (DRAM) devices"	28
"the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks"	28, 88
"the set of input control signals comprises fewer chip-select signals than does the set of output control signals"	31
"wherein the set of input control signals comprises two chip-select signals and the set of output control signals comprises four chip-select signals"	32
"two or more ranks which are selectable by a first number of chip-select signals"	39, 90
"integrated circuit element"	39, 90

Term	Relevant Claim(s)
"the at least one integrated circuit element comprising a logic element, a register, and [a] phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register"	39, 90
"receiving a plurality of input signals from the computer system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals"	39, 90
"the at least one integrated circuit element further responsive to the plurality of input signals by selecting at least one rank of the two or more ranks"	39, 90
"transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank"	39, 90
"the register (i) receives, from among the plurality of input signals, and (ii) buffers, in response to the PLL clock signal, the bank address signals and a plurality of the row address signals"	39, 90
transmits the buffered bank address signals and the buffered [plurality of] row address signals to the at least one DDR memory device of the selected at least one rank	39, 90
"the plurality of output signals corresponds to a first number of DDR memory devices arranged in the two or more ranks which are selectable by the first number of chip-select signals"	40
"the plurality of input signals corresponds to a second number of DDR memory devices arranged in ranks which are selectable by the second number of chip-select signals"	40
"simulates a virtual memory module having the second number of DDR memory devices"	40
"the at least one integrated circuit element is configured to respond to the plurality of input signals by selecting at least one rank of the two or more ranks"	50
"the plurality of DDR [memory/DRAM] devices has [at least one attribute/one or more attributes] selected from a group consisting of a number of row address bits per DDR [memory/DRAM] device, a number of column address bits per DDR [memory/DRAM] device, a number of [internal] bank[s/address bits] per DDR [memory/DRAM] device, a number of DDR [memory/DRAM] devices, a data width per DDR [memory/DRAM] device, a memory density per DDR [memory/DRAM] device, a number of ranks of DDR [memory/DRAM] devices, and a memory density per rank"	52, 62, 63, 64, 69, 73, 81
"a read-only nonvolatile memory device storing data accessible to the computer system"	52, 55
"the data characterizes the plurality of DDR memory devices as having at least one value of the at least one attribute that is different	52

Term	Relevant Claim(s)
from an actual value of the at least one attribute of the plurality of DDR memory devices"	
"the data characterizes the plurality of DDR [memory/DRAM] devices as having fewer ranks of DDR [memory/DRAM] devices than the plurality of DDR [memory/DRAM] devices actually has, and as having a greater memory density per rank than the plurality of DDR [memory/DRAM] devices actually has"	54, 65, 70, 74
"DDR dynamic random-access memory (DRAM) chip package with a bit width"	55
"the data characterizes the memory module as having fewer ranks than the first number of ranks, and as having a greater memory density per rank than the memory module actually has"	55
"means for characterizing the plurality of DDR [memory/DRAM] devices as having one or more attributes that are different from actual attributes of the plurality of DDR [memory/DRAM] devices"	56, 71, 75
"the set of input control signals corresponds to a first memory density, and the set of output control signals corresponds to a second memory density"	57
"the register comprises a plurality of register devices"	58
"the at least one row address signal and the bank address signals are (i) received by the logic element during an activate command operation and (ii) are used by the logic element for a subsequent read or write command operation"	60
"a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system"	62, 63, 64, 69, 73, 81
"the data characterizes the plurality of DDR [memory/DRAM] devices as having one or more attributes that are different from [the] one or more attributes of [the] plurality of DDR [memory/DRAM] devices"	62, 63, 64, 69, 73, 81
"the logic element responds to at least (i) a row address bit of the at least one row/column address signal, (ii) the bank signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock by generating a first number of chip-select signals of the set of output control signals"	77
"wherein operation of the register is responsive at least in part to clock signals received from the phase-lock loop device"	80
"the logic element generates a first number of chips-elect signals of the set of output control signals in response at least in part to clock signals received from the phase-lock loop device"	80
"a plurality of row/column address signals and the bank address signals are received from the computer system and buffered by the register, the register transmitting the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices"	80

Term	Relevant Claim(s)
"generation of the first number of chip-select signals of the output control signals by the logic element is based on the logic element responsive at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals received by the logic element and (iv) the clock signals received from the phase-lock loop device"	80
"the logic element responds to at least the at least one row address signal, the bank address signals, and the at least one chip-select signal of the set of input control signals and the PLL clock signal by generating a number of rank-selecting signals of the set of output control signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals"	82
"the memory module is operable to perform successive read accesses from different ranks of DDR memory devices"	83
"the memory module is operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries"	84, 87, 89, 91
"the bank address signals include bank address signals received during an activate command operation and bank address signals received during a read or write command operation subsequent to the activate command operation"	85
"and the rank-selecting signals are used for the read or write command operation"	85
"the logic element responds to at least the at least one row address signal, the bank address signals, and the at least one chip-select signal of the set of input signals and the PLL clock signal by generating a number of rank-selecting signals of the set of output signals that is greater than double or equal to double the number of chip-select signals of the set of input signals"	86
"the logic element responds to at least (i) the row address signal, (ii) the bank address signals, (iii) and the one chip-select signal of the set of input control signals and (iv) the PLL clock signal by generating a number of rank-selecting signals of the set of output signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals"	88
"the logic element responds to at least (i) the at least one row signal, (ii) the bank address signals, (iii) and the second number of chip-select signals of the plurality of input signals and (iv) the PLL clock signal by generating the first number of chip-select signals of the plurality of output signals that is greater than double or equal to double the second number of chip-select signals of the plurality of input signals"	90

2. Invalidity Under 35 U.S.C. § 112, ¶ 2

"[T]he second paragraph of § 112 contains two requirements: first, the claim must set forth what the applicant regards as his invention, and second, it must do so with sufficient particularity and distinctness, *i.e.*, the claim must be sufficiently definite." *Allen Eng'g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1348 (Fed. Cir. 2002) (internal quotation marks and alteration omitted). "Where it would be apparent to one of skill in the art, based on the specification, that the invention set forth in a claim is not what the patentee regarded as his invention," the claim is "invalid under § 112, paragraph 2." *Id.* at 1349. Several of the '912 patent Asserted Claims are invalid because it would be apparent to one of skill in the art, based on the specification, that the invention set forth in these claims are not what the patentee regarded as his invention. *Id.* These claims are invalid under the "applicant regards" prong of § 112 at least because they contain elements that differ from and/or conflict with the '912 patent's written description of the invention, or because they omit elements that one of skill in the art would understand as part of the '912 patent's invention based on the specification: 1, 3, 4, 6, 8, 10, 11, 15, 16, 18, 19, 20, 22, 24, 27, 28, 29, 31, 32, 34, 36, 37, 38, 39, 40, 41, 43, 45, 46, 47, 50, 52, 53, 54, 55, 56, 57, 58, 59, 60, 62, 63, 64, 65, 69, 70, 71, 72, 73, 74, 75, 77, 80-87, 88-89, 90-91.

Under § 112, ¶ 2, "a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014). Several of the '912 patent Asserted Claims are also invalid as indefinite under § 112, ¶ 2 because they fail to inform those skilled in the art about the scope of the invention with reasonable certainty and are indefinite.

The following limitations recited in the '912 patent Asserted Claims are indefinite in whole, in part or in combination:[6]

Term	Relevant Claim(s)
"logic element"	1, 6, 8, 15, 16, 24, 27, 28, 29, 39, 43, 45, 59, 60, 77, 80, 82, 86, 88, 90
"buffer"	1, 15, 28, 39, 77 80, 82, 86, 88, 90
"in the direction along the first side"	11, 47
"in the direction along the second side"	11, 47
"memory module connectable to a computer system"	1, 15, 16, 28, 39, 77, 80, 82, 86, 88, 90
"double-data-rate (DDR) memory devices"	1, 15, 16, 39, 77, 80, 82, 86, 88, 90
"register"	1, 8, 15, 16, 27, 28, 39, 45, 58, 72, 77, 80, 82, 86, 88, 90
"receiving a set of input [control] signals from the computer system, the set of input [control] signals comprising at least one row/column address signal, bank address signals, [and at least one/a] chip-select signal[, and an input command signal]"	1, 15, 16, 28, 77, 80, 82, 86, 88
"the set of input control signals corresponding to a second number of DDR memory devices"	1, 77, 80, 82
"generating a [set/plurality] of output [control] signals in response to the [set/plurality of input [control] signals"	1, 15, 16, 28, 39, 77, 80, 82, 86, 88, 90
"the set of output control signals corresponding to the first number of DDR memory devices"	1, 77, 80, 82
"responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices"	1, 77, 80, 82
"the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks"	1, 77, 80, 82

[6] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

Term	Relevant Claim(s)
"the phase-lock loop device operatively coupled to the plurality of DDR [memory/DRAM] devices, the logic element, and the register"	1, 15, 16, 28, 77, 80, 82, 86, 88
"in respons[e/ive] to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR [DRAM] memory devices, the logic element, and the register"	1, 15, 28, 39, 77, 82, 86, 88, 90
"the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals"	1, 15, 28, 77, 82, 86, 88
"transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices"	1, 77, 82
"the [at least one] row/column address signal received by the logic element comprises [at least one/a] row address signal received by the logic element"	1, 15, 28, 39, 77, 80, 82, 86, 90
"the plurality of row[/column] address signals received by the register are separate from the [at least one] row address signal received by the logic element"	1, 15, 28, 39, 77, 80, 82, 86, 90
"generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response to at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the [set/plurality] of input [control] signals and (iv) the PLL clock signal."	1, 15, 28, 39
"wherein the set of input control signals comprises a first number of chip-select signals and wherein the set of output control signals comprises a second number of chip-select signals"	3
"custom-designed semiconductor device"	6, 24, 29, 41
"two or more of the phase-lock loop device, the register, and the logic element are portions of a single component"	8, 27
"spaced from"	10, 11, 46, 47
"a direction along the [first/second] side"	11, 47
"the set of input signals configured to control a second number of DDR [memory/DRAM] devices"	15, 16, 28, 86, 88
"the set of output signals configured to control the first number of DDR [memory/DRAM] devices"	15, 16, 28, 86, 88
"the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks"	15, 16, 86
"transmits the buffered plurality of row/column address signals and the buffered bank address signals to the at least one DDR [memory/DRAM] device of the selected one or two ranks of the first number of ranks"	15, 28, 86, 88
"the command signal is transmitted to only one DDR memory device at a time"	16

Term	Relevant Claim(s)
"the command signal is transmitted to two ranks of the first number of ranks at a time"	18
"the command signal is transmitted to the two ranks of the first number of ranks concurrently"	20
"the set of input signals comprises a density bit which is a row address bit"	22
"the circuit is configured to store the row address bit during an activate command for a selected bank"	22
"double-data-rate (DDR) dynamic random access memory (DRAM) devices"	28
"the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks"	28, 88
"the set of input control signals comprises fewer chip-select signals than does the set of output control signals"	31
"wherein the set of input control signals comprises two chip-select signals and the set of output control signals comprises four chip-select signals"	32
"wherein the input command signal is a read signal or a write signal and the output command signal is a read signal or a write signal"	38
"a first side and second side"	39
"two or more ranks which are selectable by a first number of chip-select signals"	39, 90
"integrated circuit element"	39, 90
"the at least one integrated circuit element comprising a logic element, a register, and [a] phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register"	39, 90
"receiving a plurality of input signals from the computer system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals"	39, 90
"the at least one integrated circuit element further responsive to the plurality of input signals by selecting at least one rank of the two or more ranks"	39, 90
"transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank"	39, 90
"the register (i) receives, from among the plurality of input signals, and (ii) buffers, in response to the PLL clock signal, the bank address signals and a plurality of the row address signals"	39, 90
transmits the buffered bank address signals and the buffered [plurality of] row address signals to the at least one DDR memory device of the selected at least one rank	39, 90

Term	Relevant Claim(s)
"the plurality of output signals corresponds to a first number of DDR memory devices arranged in the two or more ranks which are selectable by the first number of chip-select signals"	40
"the plurality of input signals corresponds to a second number of DDR memory devices arranged in ranks which are selectable by the second number of chip-select signals"	40
"simulates a virtual memory module having the second number of DDR memory devices"	40
"the at least one integrated circuit element is configured to respond to the plurality of input signals by selecting at least one rank of the two or more ranks"	50
"the plurality of DDR [memory/DRAM] devices has [at least one attribute/one or more attributes] selected from a group consisting of a number of row address bits per DDR [memory/DRAM] device, a number of column address bits per DDR [memory/DRAM] device, a number of [internal] bank[s/address bits] per DDR [memory/DRAM] device, a number of DDR [memory/DRAM] devices, a data width per DDR [memory/DRAM] device, a memory density per DDR [memory/DRAM] device, a number of ranks of DDR [memory/DRAM] devices, and a memory density per rank"	52, 62, 63, 64, 69, 73, 81
"a read-only nonvolatile memory device storing data accessible to the computer system"	52, 55
"the data characterizes the plurality of DDR memory devices as having at least one value of the at least one attribute that is different from an actual value of the at least one attribute of the plurality of DDR memory devices"	52
"the data characterizes the plurality of DDR [memory/DRAM] devices as having fewer ranks of DDR [memory/DRAM] devices than the plurality of DDR [memory/DRAM] devices actually has, and as having a greater memory density per rank than the plurality of DDR [memory/DRAM] devices actually has"	54, 65, 70, 74
"DDR dynamic random-access memory (DRAM) chip package with a bit width"	55
"the data characterizes the memory module as having fewer ranks than the first number of ranks, and as having a greater memory density per rank than the memory module actually has"	55
"means for characterizing the plurality of DDR [memory/DRAM] devices as having one or more attributes that are different from actual attributes of the plurality of DDR [memory/DRAM] devices"	56, 71, 75
"the set of input control signals corresponds to a first memory density, and the set of output control signals corresponds to a second memory density"	57
"the register comprises a plurality of register devices"	58

Term	Relevant Claim(s)
"the at least one row address signal and the bank address signals are (i) received by the logic element during an activate command operation and (ii) are used by the logic element for a subsequent read or write command operation"	60
"a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system"	62, 63, 64, 69, 73, 81
"the data characterizes the plurality of DDR [memory/DRAM] devices as having one or more attributes that are different from [the] one or more attributes of [the] plurality of DDR [memory/DRAM] devices"	62, 63, 64, 69, 73, 81
"the logic element responds to at least (i) a row address bit of the at least one row/column address signal, (ii) the bank signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock by generating a first number of chip-select signals of the set of output control signals"	77
"wherein operation of the register is responsive at least in part to clock signals received from the phase-lock loop device"	80
"the logic element generates a first number of chips-elect signals of the set of output control signals in response at least in part to clock signals received from the phase-lock loop device"	80
"a plurality of row/column address signals and the bank address signals are received from the computer system and buffered by the register, the register transmitting the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices"	80
"generation of the first number of chip-select signals of the output control signals by the logic element is based on the logic element responsive at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals received by the logic element and (iv) the clock signals received from the phase-lock loop device"	80
"the logic element responds to at least the at least one row address signal, the bank address signals, and the at least one chip-select signal of the set of input control signals and the PLL clock signal by generating a number of rank-selecting signals of the set of output control signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals"	82
"the memory module is operable to perform successive read accesses from different ranks of DDR memory devices"	83
"the memory module is operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries"	84, 87, 89, 91
"the bank address signals include bank address signals received during an activate command operation and bank address signals	85

Term	Relevant Claim(s)
received during a read or write command operation subsequent to the activate command operation"	
"and the rank-selecting signals are used for the read or write command operation"	85
"the logic element responds to at least the at least one row address signal, the bank address signals, and the at least one chip-select signal of the set of input signals and the PLL clock signal by generating a number of rank-selecting signals of the set of output signals that is greater than double or equal to double the number of chip-select signals of the set of input signals"	86
"the logic element responds to at least (i) the row address signal, (ii) the bank address signals, (iii) and the one chip-select signal of the set of input control signals and (iv) the PLL clock signal by generating a number of rank-selecting signals of the set of output signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals"	88
"the logic element responds to at least (i) the at least one row signal, (ii) the bank address signals, (iii) and the second number of chip-select signals of the plurality of input signals and (iv) the PLL clock signal by generating the first number of chip-select signals of the plurality of output signals that is greater than double or equal to double the second number of chip-select signals of the plurality of input signals"	90

3. Indefiniteness Under 35 U.S.C. § 112, ¶ 6

Section 112, ¶ 6 allows a patentee to express a claim element "as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof." 35 U.S.C. § 112, ¶ 6. For such claims, the written description of the patent must disclose with sufficient particularity the corresponding structure for performing the claimed function, and it must clearly link that structure to the claimed function. *Ibormeith IP, LLC v. Mercedes-Benz USA, LLC*, 732 F.3d 1376, 1379 (Fed. Cir. 2013).

Several of the '912 patent Asserted Claims are invalid under § 112, ¶ 6 because they contain means-plus-function terms and the '912 patent fails to disclose with sufficient particularity the corresponding structure for performing the claimed function.

The following limitations recited in the '912 patent Asserted Claims are indefinite in whole, in part or in combination:[7]

Term	Relevant Claim(s)
"logic element"	All Asserted Claims
"means for characterizing the plurality of DDR [memory/DRAM] devices as having one or more attributes that are different from actual attributes of the plurality of DDR [memory/DRAM] devices"	56, 71, 75

B. U.S. Patent No. 9,858,215

Pursuant to Rule 3-3(d), Defendants hereby identify grounds of invalidity for the '215 Patent based on lack of written description under 35 U.S.C. § 112, first paragraph; lack of enablement under 35 U.S.C. § 112, first paragraph; indefiniteness under 35 U.S.C. § 112, second paragraph; and indefiniteness under 35 U.S.C. § 112, sixth paragraph. These contentions shall not be construed as an admission that any claim construction advanced by Defendants in this case is in any way inconsistent, flawed, or erroneous. Nor should these contentions prevent Defendants from advancing claim construction and/or non-infringement positions in lieu of, or in addition to, invalidity positions. Further, these contentions shall not be construed as an admission of or acquiescence to Plaintiff's purported construction of the claim language or of other positions advanced by Plaintiff during the course of this litigation. Defendants' invalidity contentions under 35 U.S.C. § 112 may depend, in part, on the Court's claim construction, as well as Plaintiff's alleged scope of the '215 patent Asserted Claims. Consequently, Defendants only identify the issues under 35 U.S.C. § 112 of which they are presently aware.

[7] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

1. Lack of Written Description and/or Enablement Under 35 U.S.C. § 112, ¶ 1

The '215 Patent does not provide sufficient written description to establish that the inventors were in possession of the alleged inventions recited in the '339 patent Asserted Claims at the time the '215 patent was filed. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010). In other words, the applicants did not describe their purported inventions in a manner that "reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *Id*. One of ordinary skill in the art would not have understood that the inventors were in possession of the full scope of the claimed apparatus and methods.

The specification of the '215 patent also does not enable one of ordinary skill in the art to make and/or use certain recited elements of the '215 patent Asserted Claims without undue experimentation. To the extent the following limitations are definite (under 35 U.S.C. § 112, ¶ 2), the application that became the '215 patent fails to sufficiently describe or enable them as required by 35 U.S.C. § 112, ¶ 1:[8]

Term	Relevant Claim(s)
"logic"	1, 8, 16, 18, 19, 20
"rank"	1, 14, 21, 26
"buffer"	1, 8, 12, 13, 14, 17, 20, 21, 26
"register"	1
"a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system"	1
"a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command"	1

[8] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

Term	Relevant Claim(s)
"wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command"	1
"a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus"	1
"logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer"	1
"wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals"	1
"a plurality of edge connections coupled to the memory bus"	21
"receiving at one or more circuits coupled to the printed circuit board a first set of input command and address signals representing a first memory command from the memory controller via the memory bus"	21
"generating a first set of output command and address signals in response to the first set of input command and address signals, the first set of output command and address signals selecting the first rank to receive or output the first data burst"	21
"receiving at the one or more circuits a second set of input command and address signals representing a second memory command from the memory controller via the memory bus, the second memory command to cause the memory module to receive or output a second data burst"	21
"generating a second set of output command and address signals in response to the second set of input command and address signals, the second set of output command and address signals selecting the second rank to receive or output the second data burst"	21
"in response to the first memory command, providing first control signals to a buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer;"	21
"and in response to the second memory command, providing second control signals to the buffer to enable communication of the	21

Term	Relevant Claim(s)
second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals"	
"wherein the buffer is configured to isolate both the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory controller"	2
"wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of each of the plurality of memory integrated circuits"	3
"an SPD device that reports an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of each of the plurality of memory integrated circuits"	4
"wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits"	5
"determining a latency value, wherein the communication of the first data burst between the at least one first memory integrated circuit and the memory controller is enabled in accordance with the latency value"	6
"wherein the memory module is further coupled to the memory controller using an on-die-termination (ODT) bus, wherein each of the plurality of memory devices includes an ODT circuit, the memory module further comprising a termination circuit external to any of the plurality of memory devices, wherein the termination circuit is coupled to the ODT bus and to the ODT circuit of at least one of the plurality of memory devices, wherein the termination circuit is configured to provide external termination of the at least one of the plurality of memory devices in response to an ODT signal on the ODT bus, and wherein the ODT circuit in the at least one of the plurality of memory devices is disabled"	7
"wherein the buffer comprises combinatorial logic, registers, and logic pipelines, and is configured to register an additional clock cycle for transferring the first data burst or the second data burst through the buffer"	8
"wherein the first memory command includes at least one first chip select signal and the second memory command includes at least one second chip select signal"	9
"wherein the memory module produces at least third and fourth chip select signals in response to the first memory command, the third chip select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data	10

Term	Relevant Claim(s)
signals in response to the first memory command, the fourth chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command"	
"wherein the memory module produces at least fifth and sixth chip select signals in response to the second memory command, the fifth chip select signal being provided to the at least one first memory integrated circuit and having a non-active value to keep the at least one first memory integrated circuit from receiving or outputting data signals in response to the first memory command, the sixth chip select signal being provided to the at least one second memory integrated circuit and having an active value to cause the at least one second memory integrated circuit to receive or output data signals in response to the second memory command"	11
"wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and wherein the memory module outputs the first data burst together with a first burst of data strobe signals in response to the first read command, wherein memory module outputs the second data burst together with a second burst of data strobe signals in response to the second read command, wherein the second data burst follows the first data burst on the memory bus, and wherein the buffer is configured to prevent the first burst of data strobe signals and the second burst of data strobe signals from colliding with each other"	12
"wherein each of the first burst of data strobe signals and the second burst of data strobe signals includes a pre-amble interval and a post-amble interval, and wherein the buffer is configured to combine the first burst of data strobe signals and the second burst of data strobe signals into a combined burst of data strobe signals that does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals"	13
"wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is selected to communicate data with the memory controller"	14
"the at least one of the circuit components is configured to provide the first data path in response to the first control signals, and is configured to provide the second data path in response to the second control signals"	15
"wherein the logic is configured to enable the communication of the first data burst between the at least one first memory integrated	16

Term	Relevant Claim(s)
circuit and the memory controller in accordance with a latency value"	
"wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the first data burst through the buffer"	17
"wherein the logic is further configured to determine the latency value"	18
"wherein the logic is further configured to enable the communication of the second data burst between the at least one second memory integrated circuit and the memory controller in accordance with the latency value"	19
"wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the second data burst through the buffer"	20
"isolating the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory system"	22
"wherein the first set of input command and address signals include at least one input chip-select signal, the method further comprising generating a first chip select signal and a second chip select signal in response to the first set of input command and address signals, the first chip-select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the second chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command"	23
"wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of the memory integrated circuits"	24
"reporting an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of the memory integrated circuits"	25
"wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is caused to communicate data with the memory controller"	26
"wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits"	27

Term	Relevant Claim(s)
"wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and wherein the memory module outputs the first data burst together with a first burst of data strobe signals in response to the first read command, wherein the memory module outputs the second data burst together with a second burst of data strobe signals in response to the second read command, wherein the second data burst follows the first data burst on the memory bus, the method further comprising combining the first burst of data strobe signals and the second burst of data strobes to form a third burst of data strobe signals on the memory bus"	28
"wherein each of the first burst of data strobe signals and the second burst of data strobe signals includes a pre-amble interval and a post-amble interval, and wherein the third burst of data strobes does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals"	29

2. Invalidity Under 35 U.S.C. § 112, ¶ 2

"[T]he second paragraph of § 112 contains two requirements: first, the claim must set forth what the applicant regards as his invention, and second, it must do so with sufficient particularity and distinctness, *i.e.*, the claim must be sufficiently definite." *Allen Eng'g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1348 (Fed. Cir. 2002) (internal quotation marks and alteration omitted). "Where it would be apparent to one of skill in the art, based on the specification, that the invention set forth in a claim is not what the patentee regarded as his invention," the claim is "invalid under § 112, paragraph 2." *Id.* at 1349. Several of the '215 patent Asserted Claims are invalid because it would be apparent to one of skill in the art, based on the specification, that the invention set forth in these claims are not what the patentee regarded as his invention. *Id.* These claims are invalid under the "applicant regards" prong of § 112 at least because they contain elements that differ from and/or conflict with the '215 patent's written description of the invention, or because they omit elements that one of skill in

the art would understand as part of the '215 patent's invention based on the specification: 1, 2-20, 21-29.

Under § 112, ¶ 2, "a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014). Several of the '215 patent Asserted Claims are also invalid as indefinite under § 112, ¶ 2 because they fail to inform those skilled in the art about the scope of the invention with reasonable certainty and are indefinite.

The following limitations recited in the '215 patent Asserted Claims are indefinite in whole, in part or in combination:[9]

Term	Relevant Claim(s)
"logic"	1, 8, 16, 18, 19, 20
"a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command"	1
"wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command;"	1
"a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus"	1
"logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer,"	1

[9] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

Term	Relevant Claim(s)
"wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals"	1
"receiving at one or more circuits coupled to the printed circuit board a first set of input command and address signals representing a first memory command from the memory controller via the memory bus"	21
"generating a first set of output command and address signals in response to the first set of input command and address signals, the first set of output command and address signals selecting the first rank to receive or output the first data burst;"	21
"receiving at the one or more circuits a second set of input command and address signals representing a second memory command from the memory controller via the memory bus, the second memory command to cause the memory module to receive or output a second data burst"	21
"generating a second set of output command and address signals in response to the second set of input command and address signals, the second set of output command and address signals selecting the second rank to receive or output the second data burst"	21
"in response to the first memory command, providing first control signals to a buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer"	21
"and in response to the second memory command, providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals"	21
"wherein the buffer is configured to isolate both the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory controller"	2
"an SPD device that reports an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of each of the plurality of memory integrated circuits"	4
"determining a latency value, wherein the communication of the first data burst between the at least one first memory integrated circuit and the memory controller is enabled in accordance with the latency value"	6

Term	Relevant Claim(s)
"wherein the buffer comprises combinatorial logic, registers, and logic pipelines, and is configured to register an additional clock cycle for transferring the first data burst or the second data burst through the buffer"	8
"wherein the memory module produces at least fifth and sixth chip select signals in response to the second memory command, the fifth chip select signal being provided to the at least one first memory integrated circuit and having a non-active value to keep the at least one first memory integrated circuit from receiving or outputting data signals in response to the first memory command, the sixth chip select signal being provided to the at least one second memory integrated circuit and having an active value to cause the at least one second memory integrated circuit to receive or output data signals in response to the second memory command"	11
"the at least one of the circuit components is configured to provide the first data path in response to the first control signals, and is configured to provide the second data path in response to the second control signals"	15
"wherein the logic is configured to enable the communication of the first data burst between the at least one first memory integrated circuit and the memory controller in accordance with a latency value"	16
"wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the first data burst through the buffer"	17
"wherein the logic is further configured to determine the latency value"	18
"wherein the logic is further configured to enable the communication of the second data burst between the at least one second memory integrated circuit and the memory controller in accordance with the latency value"	19
"wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the second data burst through the buffer"	20
"isolating the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory system"	22
"wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of the memory integrated circuits"	24
"wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is caused to communicate data with the memory controller"	26

Term	Relevant Claim(s)
"wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits"	27

3. Indefiniteness Under 35 U.S.C. § 112, ¶ 6

Section 112, ¶ 6 allows a patentee to express a claim element "as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof." 35 U.S.C. § 112, ¶ 6. For such claims, the written description of the patent must disclose with sufficient particularity the corresponding structure for performing the claimed function, and it must clearly link that structure to the claimed function. *Ibormeith IP, LLC v. Mercedes-Benz USA, LLC*, 732 F.3d 1376, 1379 (Fed. Cir. 2013).

Several of the '215 patent Asserted Claims are invalid under § 112, ¶ 6 because they contain means-plus-function terms and the '215 patent fails to disclose with sufficient particularity the corresponding structure for performing the claimed function.

The following limitations recited in the '215 patent Asserted Claims are indefinite in whole, in part or in combination:[10]

Term	Relevant Claim(s)
"logic"	1-20
"buffer"	All Asserted Claims

C. U.S. Patent No. 11,093,417

Pursuant to Rule 3-3(d), Defendants hereby identify grounds of invalidity for the '417 Patent based on lack of written description under 35 U.S.C. § 112, first paragraph; lack of enablement under 35 U.S.C. § 112, first paragraph; indefiniteness under 35 U.S.C. § 112, second

[10] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

paragraph; and indefiniteness under 35 U.S.C. § 112, sixth paragraph. These contentions shall not be construed as an admission that any claim construction advanced by Defendants in this case is in any way inconsistent, flawed, or erroneous. Nor should these contentions prevent Defendants from advancing claim construction and/or non-infringement positions in lieu of, or in addition to, invalidity positions. Further, these contentions shall not be construed as an admission of or acquiescence to Plaintiff's purported construction of the claim language or of other positions advanced by Plaintiff during the course of this litigation. Defendants' invalidity contentions under 35 U.S.C. § 112 may depend, in part, on the Court's claim construction, as well as Plaintiff's alleged scope of the '417 patent Asserted Claims. Consequently, Defendants only identify the issues under 35 U.S.C. § 112 of which they are presently aware.

1. Lack of Written Description and/or Enablement Under 35 U.S.C. § 112, ¶ 1

The '417 patent does not provide sufficient written description to establish that the inventors were in possession of the alleged inventions recited in the '417 patent Asserted Claims at the time the '417 patent was filed. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010). In other words, the applicants did not describe their purported inventions in a manner that "reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *Id*. One of ordinary skill in the art would not have understood that the inventors were in possession of the full scope of the claimed apparatus and methods.

The specification of the '417 patent also does not enable one of ordinary skill in the art to make and/or use certain recited elements of the '417 patent Asserted Claims without undue experimentation. To the extent the following limitations are definite (under 35 U.S.C. § 112,

¶ 2), the application that became the '417 patent fails to sufficiently describe or enable them as required by 35 U.S.C. § 112, ¶ 1:[11]

Term	Relevant Claim(s)
"logic"	1, 6, 7,
"circuitry"	1, 2, 3, 6, 11, 12, 13, 15
"a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;"	1
"logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals,"	1
"the set of input address and control signals including a plurality of input chip select signals and other input address and control signals,"	1
"the plurality of input chip select signals including one chip select signal having an active signal value and one or more other input chip select signals each having a non-active signal value,"	1
"the set of registered address and control signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals and other registered address and control signals corresponding to respective ones of the other input address and control signals,"	1
"the plurality of registered chip select signals including one registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value,"	1
"wherein the logic is further configurable to output data buffer control signals in response to the read or write memory command;"	1
"wherein the plurality of N-bit wide ranks correspond to respective ones of the plurality of registered chip select signals such that each of the plurality of registered chip select signals is received by memory devices one respective N-bit wide rank of the plurality of N-bit-wide ranks,"	1
"wherein one of the plurality of N-bit wide ranks including memory devices receiving the registered chip select signal having the active signal value and the other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command;"	1

[11] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

Term	Relevant Claim(s)
"circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module;"	1
"wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices."	1
"wherein each of the memory devices has a corresponding load, and the circuitry is configured to isolate the loads of the memory devices from the memory bus."	2
"wherein the burst of N-bit wide data signals includes a set of consecutively transmitted data bits for each data signal line in the memory bus, and wherein the set of consecutively transmitted data bits are successively transferred through the circuitry in response to the data buffer control signals."	3
"wherein each of the memory devices is 4-bits wide, and wherein each of the plurality of ranks is 64-bits or 72-bits wide and includes 16 or 18 memory devices configured in pairs."	4
"wherein the memory devices are organized in four ranks and the set of input address and control signals include four chip select signals, one for each of the four ranks."	5
"wherein the circuitry includes logic pipelines configurable to enable the data transfers between the memory devices and the memory bus through the circuitry."	6
"wherein the logic is further configured to report the overall CAS latency to the memory controller in response to a mode register set command received from the memory controller."	7
"wherein the memory module has a specified data rate, and wherein the burst of N-bit wide data signals are transferred between the one of the plurality of N-bit wide ranks and the memory controller at the specified data rate."	8
"further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay."	9
"wherein the memory devices are dynamic random access memory devices configured to operate synchronously with the clock signal, and wherein each memory device in the one of the plurality of N-bit wide ranks is configured to receive or output a respective set of	10

Term	Relevant Claim(s)
bits of the burst of N-bit wide data signals on both edges of each of a respective set of data strobes."	
"wherein the circuitry includes data paths, and wherein the circuitry is configurable to enable the data paths in response to the data buffer control signals so that the burst of N-bit wide data signals are transferred via the data paths."	11
"wherein the data paths are disabled when no data signals associated with any memory command are being transferred through the circuitry."	12
"wherein each of the memory devices has a corresponding load, and the circuitry is configured to isolate the loads of the memory devices from the memory bus."	13
"wherein the memory module has a specified data rate, and wherein the burst of N-bit wide data signals are transferred through the data paths at the specified data rate."	14
"wherein the read or write command is a write memory command, wherein the burst of N-bit wide data signals include a respective series of write data bits received by the circuitry from a respective one of the data signal lines, and wherein the respective series of write data bits are successively transferred via a respective one of the data paths."	15

2. Invalidity Under 35 U.S.C. § 112, ¶ 2

"[T]he second paragraph of § 112 contains two requirements: first, the claim must set forth what the applicant regards as his invention, and second, it must do so with sufficient particularity and distinctness, *i.e.*, the claim must be sufficiently definite." *Allen Eng'g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1348 (Fed. Cir. 2002) (internal quotation marks and alteration omitted). "Where it would be apparent to one of skill in the art, based on the specification, that the invention set forth in a claim is not what the patentee regarded as his invention," the claim is "invalid under § 112, paragraph 2." *Id.* at 1349. Several of the '417 patent Asserted Claims are invalid because it would be apparent to one of skill in the art, based on the specification, that the invention set forth in these claims are not what the patentee regarded as his invention. *Id.* These claims are invalid under the "applicant regards" prong of

§ 112 at least because they contain elements that differ from and/or conflict with the '417 patent's written description of the invention, or because they omit elements that one of skill in the art would understand as part of the '417 patent's invention based on the specification: 1, 2-20, 21-29.

Under § 112, ¶ 2, "a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc*., 572 U.S. 898, 901 (2014). Several of the '417 patent Asserted Claims are also invalid as indefinite under § 112, ¶ 2 because they fail to inform those skilled in the art about the scope of the invention with reasonable certainty and are indefinite.

The following limitations recited in the '417 patent Asserted Claims are indefinite in whole, in part or in combination:[12]

Term	**Relevant Claim(s)**
"logic"	1, 6, 7,
"circuitry"	1, 2, 3, 6, 11, 12, 13, 15
"logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals,"	1
"the set of input address and control signals including a plurality of input chip select signals and other input address and control signals,"	1
"the plurality of input chip select signals including one chip select signal having an active signal value and one or more other input chip select signals each having a non-active signal value,"	1
"the set of registered address and control signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals and other registered address and control signals corresponding to respective ones of the other input address and control signals,"	1

[12] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

Term	Relevant Claim(s)
"the plurality of registered chip select signals including one registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value,"	1
"wherein the plurality of N-bit wide ranks correspond to respective ones of the plurality of registered chip select signals such that each of the plurality of registered chip select signals is received by memory devices one respective N-bit wide rank of the plurality of N-bit-wide ranks,"	1
"wherein one of the plurality of N-bit wide ranks including memory devices receiving the registered chip select signal having the active signal value and the other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command;"	1
"circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module;"	1
"wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices."	1
"wherein the burst of N-bit wide data signals includes a set of consecutively transmitted data bits for each data signal line in the memory bus, and wherein the set of consecutively transmitted data bits are successively transferred through the circuitry in response to the data buffer control signals."	3
"wherein the circuitry includes logic pipelines configurable to enable the data transfers between the memory devices and the memory bus through the circuitry."	6
"wherein the logic is further configured to report the overall CAS latency to the memory controller in response to a mode register set command received from the memory controller."	7
"further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay."	9
"wherein the circuitry includes data paths, and wherein the circuitry is configurable to enable the data paths in response to the data buffer control signals so that the burst of N-bit wide data signals are transferred via the data paths."	11

Term	Relevant Claim(s)
"wherein the data paths are disabled when no data signals associated with any memory command are being transferred through the circuitry."	12
"wherein each of the memory devices has a corresponding load, and the circuitry is configured to isolate the loads of the memory devices from the memory bus."	13
"wherein the read or write command is a write memory command, wherein the burst of N-bit wide data signals include a respective series of write data bits received by the circuitry from a respective one of the data signal lines, and wherein the respective series of write data bits are successively transferred via a respective one of the data paths."	15

3. Indefiniteness Under 35 U.S.C. § 112, ¶ 6

Section 112, ¶ 6 allows a patentee to express a claim element "as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof." 35 U.S.C. § 112, ¶ 6. For such claims, the written description of the patent must disclose with sufficient particularity the corresponding structure for performing the claimed function, and it must clearly link that structure to the claimed function. *Ibormeith IP, LLC v. Mercedes-Benz USA, LLC*, 732 F.3d 1376, 1379 (Fed. Cir. 2013).

Several of the '417 patent Asserted Claims are invalid under § 112, ¶ 6 because they contain means-plus-function terms and the '417 patent fails to disclose with sufficient particularity the corresponding structure for performing the claimed function.

The following limitations recited in the '417 patent Asserted Claims are indefinite in whole, in part or in combination:[13]

Term	Relevant Claim(s)
"logic"	1, 6, 7
"circuity"	1, 2, 3, 6, 11, 12, 13, 15

[13] Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

product, which constitutes a prior art system, is available for inspection in the Atlanta, Georgia office of Fish & Richardson, P.C. References that were cited during prosecution of the Asserted Patents may not be contained in Defendants' production as they are not required to be under the local patent rules. Defendants' search for prior art references, additional documentation, and/or corroborating evidence concerning prior art systems and devices is ongoing. Accordingly, Defendants reserve the right to supplement their production as Defendants obtain additional prior art references, documentation, and/or corroborating evidence concerning invalidity during the course of discovery.

Defendants reserve the right to supplement their P. R. 3-4 document production pursuant to the Patent Local Rules and the orders of the Court.

Date: April 13, 2023

Respectfully submitted,

/s/ Daniel A. Tishman

Ruffin B. Cordell
TX Bar No. 04820550
cordell@fr.com
Michael J. McKeon
D.C. Bar No. 459780
mckeon@fr.com
Lauren A. Degnan
D.C. Bar No. 452421
degnan@fr.com
Daniel A. Tishman
DC Bar No. 1013923
tishman@fr.com
FISH & RICHARDSON P.C.
1000 Maine Avenue, SW
Washington, DC 20024
Telephone: (202) 783-5070
Facsimile: (202) 783-2331

Francis J. Albert
CA Bar No. 247741
albert@fr.com